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OCTOBER 1983

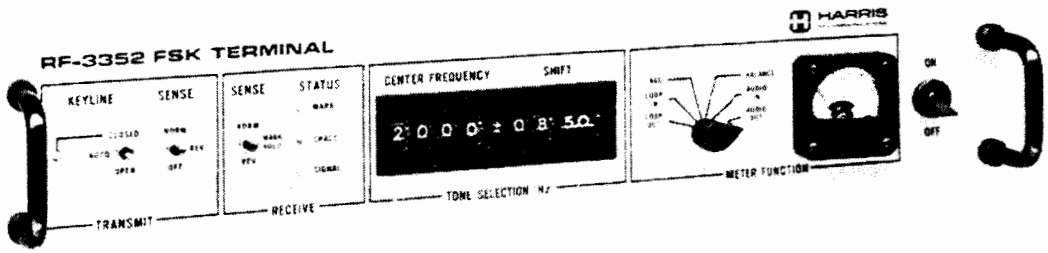
HARRIS

RF COMMUNICATIONS

RF-3352

FSK TERMINAL

INSTRUCTION MANUAL



HARRIS

LIMITED ONE YEAR WARRANTY
HARRIS CORPORATION (RF COMMUNICATIONS GROUP)

FROM HARRIS TO YOU – This warranty is extended to the original buyer and applies to all Harris Corporation, RF Communications Group equipment purchased and employed for the service normally intended, except those products specifically excluded.

WHAT WE WILL DO – If your Harris Corporation, RF Communications Group equipment purchased from us for use outside the United States fails in normal use because of a defect in workmanship or materials within one year from the date of shipment, we will repair or replace (at our option) the equipment or part without charge to you, at our factory. If the product was purchased for use in the United States, we will repair or replace (at our option) the equipment or part without charge to you at our Authorized Repair Center or factory.

WHAT YOU MUST DO – You must notify us promptly of a defect within one year from date of shipment. Assuming that Harris concurs that the complaint is valid, and is unable to correct the problem without having the equipment shipped to Harris:

- Customers with equipment purchased for use outside the United States will be supplied with information for the return of the defective equipment or part to our factory in Rochester, NY, U.S.A., for repair or replacement. You must prepay all transportation, insurance, duty and customs charges. We will pay for return to you of the repaired/replaced equipment or part, C.I.F. destination; you must pay any duty, taxes or customs charges.
- Customers with equipment purchased for use in the United States must obtain a Return Authorization Number, properly pack, insure, prepay the shipping charges and ship the defective equipment or part to our factory or to the Authorized Warranty Repair Center indicated by us.

Harris Corporation
RF Communications Group
Customer Service
1680 University Avenue
Rochester, NY 14610, U.S.A.

Telephone: (716) 244-5830
Telex: 240313
Cable: RFCOM

Harris will repair or replace the defective equipment or part and pay for its return to you, provided the repair or replacement is due to a cause covered by this warranty.

WHAT IS NOT COVERED – We regret that we cannot be responsible for:

- Defects or failures caused by buyer or user abuse or misuse.
- Defects or failures caused by unauthorized attempts to repair or alter the equipment in any way.
- Consequential damages incurred by a buyer or user from any cause whatsoever, including, but not limited to transportation, non-Harris repair or service costs, downtime costs, costs for substituting equipment or loss of anticipated profits or revenue.
- The performance of the equipment when used in combination with equipment not purchased from Harris.
- HARRIS MAKES NO OTHER WARRANTIES BEYOND THE EXPRESS WARRANTY AS CONTAINED HEREIN. ALL EXPRESS OR IMPLIED WARRANTIES OF FITNESS FOR A PARTICULAR PURPOSE OR MERCHANTABILITY ARE EXCLUDED.

SERVICE WARRANTY – Any repair service performed by Harris under this limited warranty is warranted to be free from defects in material or workmanship for sixty days from date of repair. All terms and exclusions of this limited warranty apply to the service warranty.

IMPORTANT – Customers who purchased equipment for use in the United States must obtain a Return Authorization Number before shipping the defective equipment to us. Failure to obtain a Return Authorization Number before shipment may result in a delay in the repair/replacement and return of your equipment.

IF YOU HAVE ANY QUESTIONS – Concerning this warranty or equipment sales or services, please contact our Customer Service Department.

SPARE PARTS KITS AND MOUNTING OPTIONS

Listed below are the spare parts kits and mounting options available from Harris Corporation for use with the equipment described in this manual. To order any of these items, or to obtain more information concerning them, write to:

HARRIS CORPORATION
RF Communications Division
Rochester, New York
14610 U.S.A.

ATTN: MARKETING DEPARTMENT

or call: (716) 244-5830, and ask for Marketing Department

When placing an order, please specify the model number.

We will be happy to answer any questions you may have regarding these or any other items we manufacture. We also welcome your evaluation of our equipment and suggestions for other accessory items or spare parts.

HARRIS
RF COMMUNICATIONS

Spares Kits for the RF-3352 FSK Terminal

Kit Model and Part Number	Name	Kit Description/Content
RF-3352 (RSK). Part No. 1001-0280	RF-3352 Running Spares Kit	This kit comprises the field-replaceable 1/8 Ampere fuses that may be consumed during equipment installation and setup.
RF-3352 (OSK) Part No. 1001-0281	RF-3352 Operational Spares Kit	This kit contains those items that will allow the unit to be repaired at the highest practical level of assembly (thus minimizing "down" or "off the air" time). The kit includes a complete set of assemblies and subassemblies, and piece parts for items impractical to repair by assembly or sub-assembly replacement (such as switches and meters).

Mounting Options Available for the RF-3352 FSK Terminal

Model Designation	Part Number	Option Contents/Nomenclature
RF-3352-1	6918-0011 6918-0010 Z13-0005-054 6918-1020	FSK Terminal, Slide Mounted RF-3352 FSK Terminal Chassis Slide Slide Mounting Bracket
RF-3352-2	6918-0012 6918-0010 Z13-0005-054 6918-0120	FSK Terminal, Stack Mounted RF-3352 FSK Terminal Chassis Slide Stacking Bracket
RF-3352-3	6918-0013 6918-0010 6918-1005	FSK Terminal, Desk Top RF-3352 FSK Terminal Desk Top Cabinet

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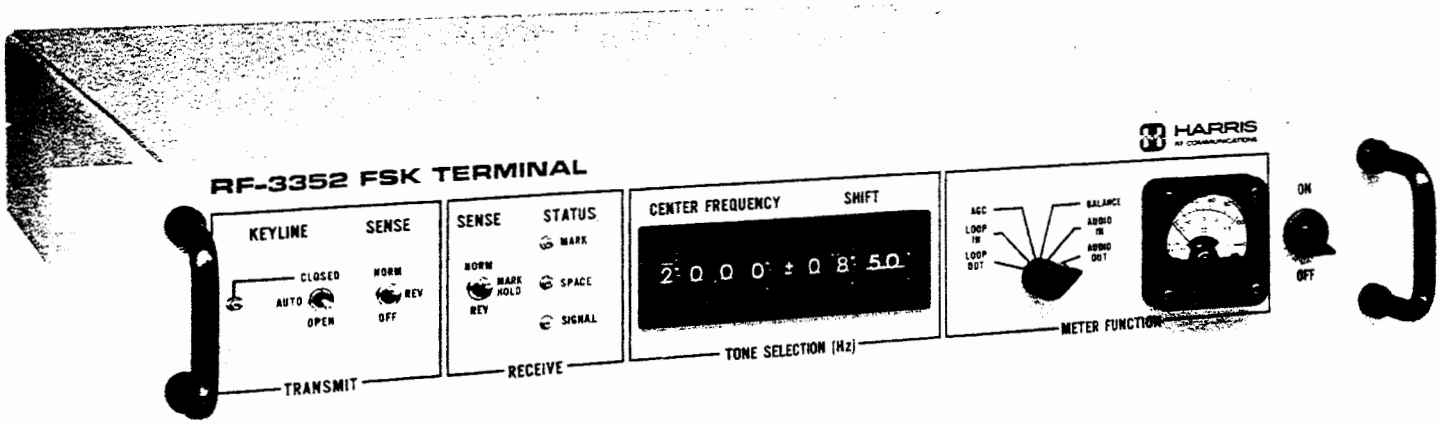


Figure 1-1. Model RF-3352 FSK Terminal

SECTION 1

INTRODUCTION

1.1 MANUAL SCOPE AND GENERAL DESCRIPTION

This technical publication provides the instructions required to operate and maintain the Model RF-3352 FSK Terminal, Part No. 6918-1100 (see Figure 1-1). This equipment is manufactured by the Harris Corporation, RF Communications Division, 1700 University Avenue, Rochester, New York 14610, United States of America.

The RF-3352 FSK Terminal provides for two-way operation of radio teleprinter equipment over a radio link. The unit contains three major functional sections, a Modulator (Keyer), a Demodulator (Converter), and a data Interface Pwb Assembly.

For modulation, Serial NRZ (No Return Zero) data, in either RS-232 or Current Loop format, is accepted by the Interface Pwb, converted to internal logic levels, and transferred to the Modulator Pwb. The modulator encodes the data into two FSK audio subcarriers which are then transmitted via radio.

The Demodulator Pwb transforms similar FSK subcarriers into a Serial NRZ data stream and, via the Interface Pwb, makes the data available to terminal equipment in either RS-232 or Current Loop format.

The Current Loop Drivers can be operated with either internal or external loop supplies. The internal loop supply output is available at the unit's rear connector.

1.2 TECHNICAL CHARACTERISTICS

Table 1-1 is a list of Technical Characteristics applicable to the RF-3352 FSK Terminal.

1.3 SPARE PARTS KITS AND MOUNTING OPTIONS

Refer to the front of this manual for a listing of spare parts kits and mounting options for the RF-3352 FSK Terminal.

Table 1-1. RF-3352 FSK TERMINAL TECHNICAL CHARACTERISTICS

Teletypewriter Input (Current Loop Receiver)	EIA RS-232C CCITT V.24/V.28 20 mA to 80 mA, Neutral 20 mA to 60 mA, Polar
Teletypewriter Output (Current Loop Driver)	EIA RS-232C CCITT V.24/V.28 20 mA to 80 mA Neutral 20 mA to 60 mA Polar

Table 1-1. RF-3352 FSK TERMINAL TECHNICAL CHARACTERISTICS (Cont)

Radio Interface	Center Frequency: 270 Hz to 3400 Hz in 5 Hz steps Shift Frequency: 0 to ±597.5 Hz in ±2.5 Hz steps Stability: Better than 0.1% Level: 0 dBm to -30 dBm, transmit ±10 dBm to -40 dBm, receive Impedence: 600 ohms, balanced
Baud Rate	50 to 150 Baud
Clear To Send Delay	Continually adjustable over a 0.1 second to 2.5 seconds range. Factory set at 1.0 second.
Traffic Detector Release Time	Adjustable from 0.4 second to 2.5 seconds following the final data state transmission. Factory set at 1.0 second.
LED Indicators	RECEIVE STATUS—MARK RECEIVE STATUS—SPACE RECEIVE STATUS—SIGNAL TRANSMIT KEYLINE—CLOSED
Tone Selection	TONE SELECTION (Hz) CENTER FREQUENCY TONE SELECTION (Hz)—SHIFT
Meter Functions (Operator Selectable)	LOOP OUT LOOP IN AGC BALANCE AUDIO IN AUDIO OUT
Power Requirements	115 VAC/230 VAC ±10%; 47 to 63 Hz, Single Phase 25 Volt-Amperes
Operating Temperature	Operation: O°C to 50°C (32°F to 122°F) Storage: 30°C to 70°C (75.6 to 158°F
Physical Dimensions	8.9 cm H x 48.3 cm W x 47 cm D (3.5 in. H x 19 in. W x 18.5 in. D)
Weight	6.8 kg (15 lb.)

Table 1-1. RF-3352 FSK TERMINAL TECHNICAL CHARACTERISTICS (Cont.)

Additional Characteristics	Reverse Sensing RS-232 Override (permits RS-232 data entry without full handshake) Auto-start Auto-start Override Traffic Detector Diversity Combining Full RS-232C Protocol

SECTION 2

INSTALLATION

2.1 INTRODUCTION

This section contains installation, electrical interconnection, emergency shutdown and adjustment instructions for the RF-3352 FSK Terminal.

2.2 UNPACKING AND INSPECTION INSTRUCTIONS

No special unpacking instructions apply. Make sure that the accessories shipped with the terminal are present and accounted for (refer to Table 2-1 for a list of the accessories). Inspect equipment for damage incurred during shipment. Report damage to nearest responsible authority for disposition.

2.3 MECHANICAL INSTALLATION/REPLACEMENT OF DAMAGED ASSEMBLIES

No special installation instructions apply. In the event that any of the terminals assemblies have to be replaced, refer to the applicable area of Section 5 of this manual.

2.4 RF-3352 FSK TERMINAL ELECTRICAL INTERCONNECTION

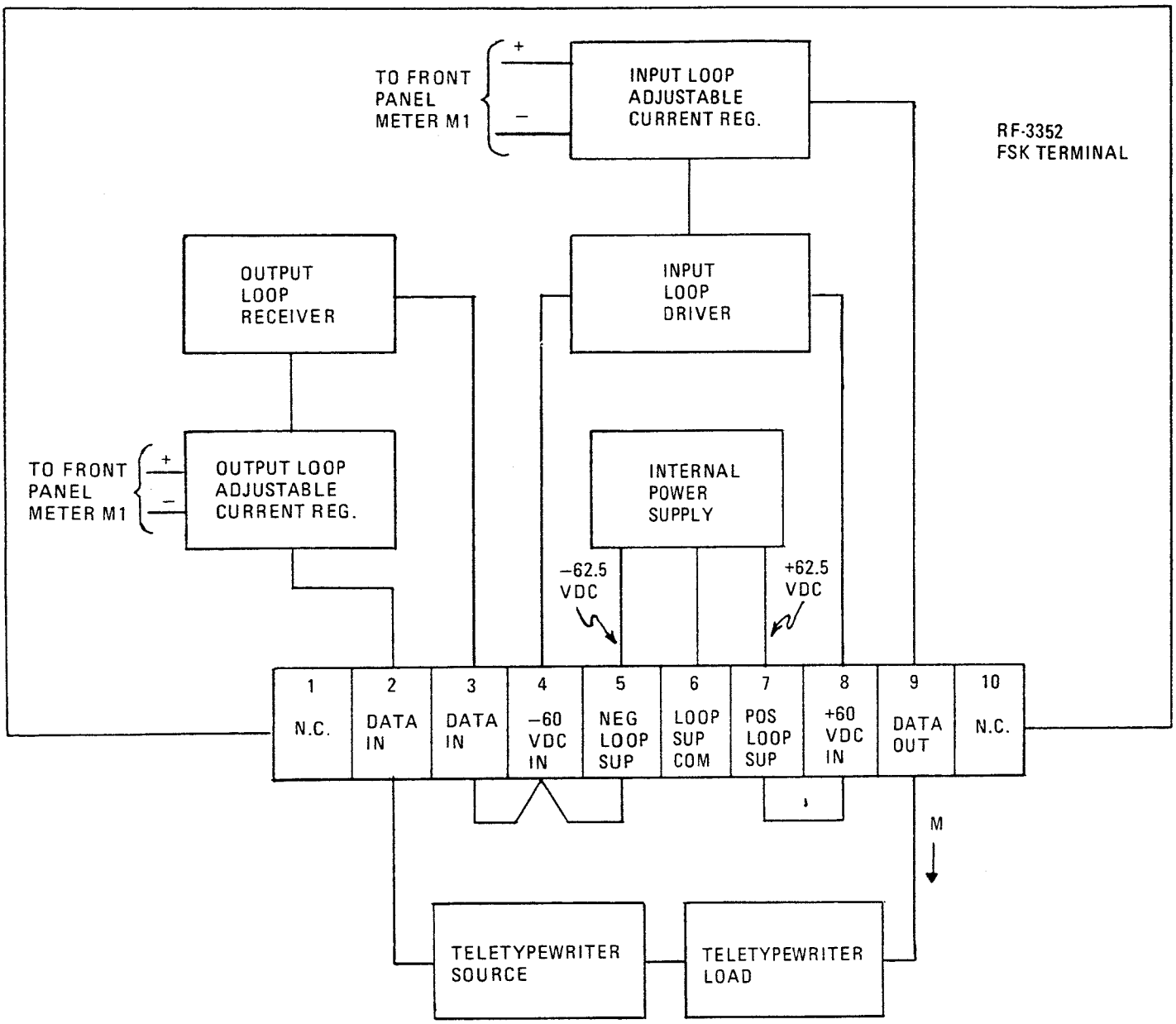
NOTE

Figures 2-1 through 2-3 comprise various interconnection diagrams. In each illustration, the interconnection is shown using the FSK Terminal's internal loop supply. Since this supply is connected to the terminal's driver and receiver circuits only via external connection. External loop power supplies may be substituted if desired.

Figure 2-1 shows the RF-3352 FSK Terminal interconnection and operational discipline for Neutral Mode-Common Loop (Half Duplex) operation. The operational discipline given must be complied with to ensure proper operation in this mode.

Figure 2-2 shows the RF-3352 FSK Terminal interconnection for Neutral Mode - Independent Loop (Full Duplex) operation.

Figure 2-3 shows the RF-3352 FSK Terminal interconnection for Polar Mode - Independent Loop (Full Duplex) operation.



OPERATIONAL DISCIPLINE

A. TRANSMISSION
   1. INPUT LOOP DRIVER MUST BE IN MARK HOLD STATE
   2. FRONT PANEL TRANSMIT-KEYLINE SWITCH MUST BE IN EITHER "CLOSED" OR "AUTO" POSITION.

B. RECEPTION
   1. TELETYPEWRITER SOURCE MUST BE IN MARK HOLD STATE
   2. FRONT PANEL TRANSMIT-KEYLINE SWITCH MUST BE IN "OPEN" POSITION

Figure 2-1. RF-3352 FSK Terminal/Teletypewriter Interconnection and Operational Discipline - Neutral Mode - Common Loop (Half Duplex)

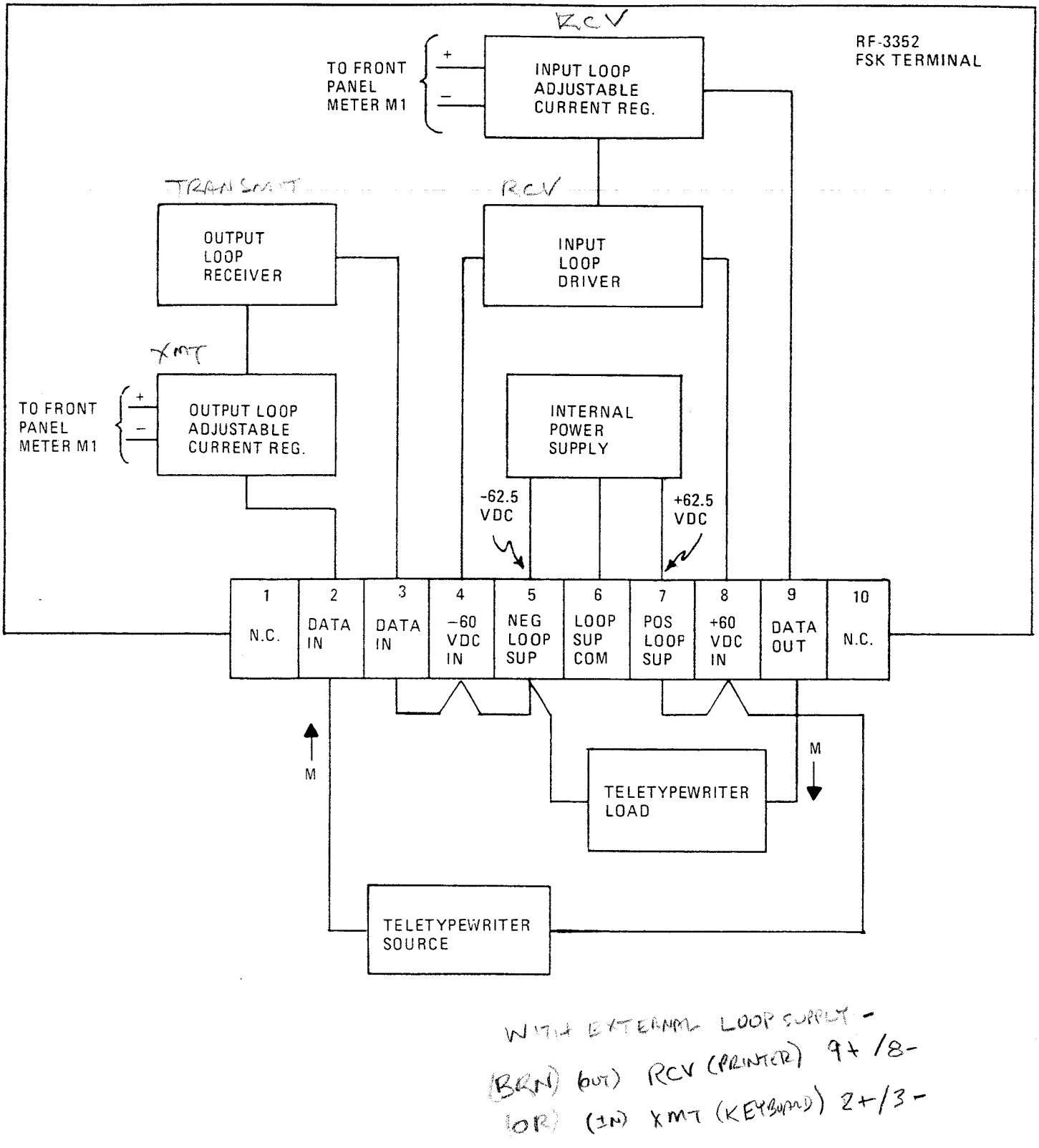


Figure 2-2. RF-3352 FSK Terminal/Teletypewriter Interconnection - Neutral Mode - Independent Loops (Full Duplex)

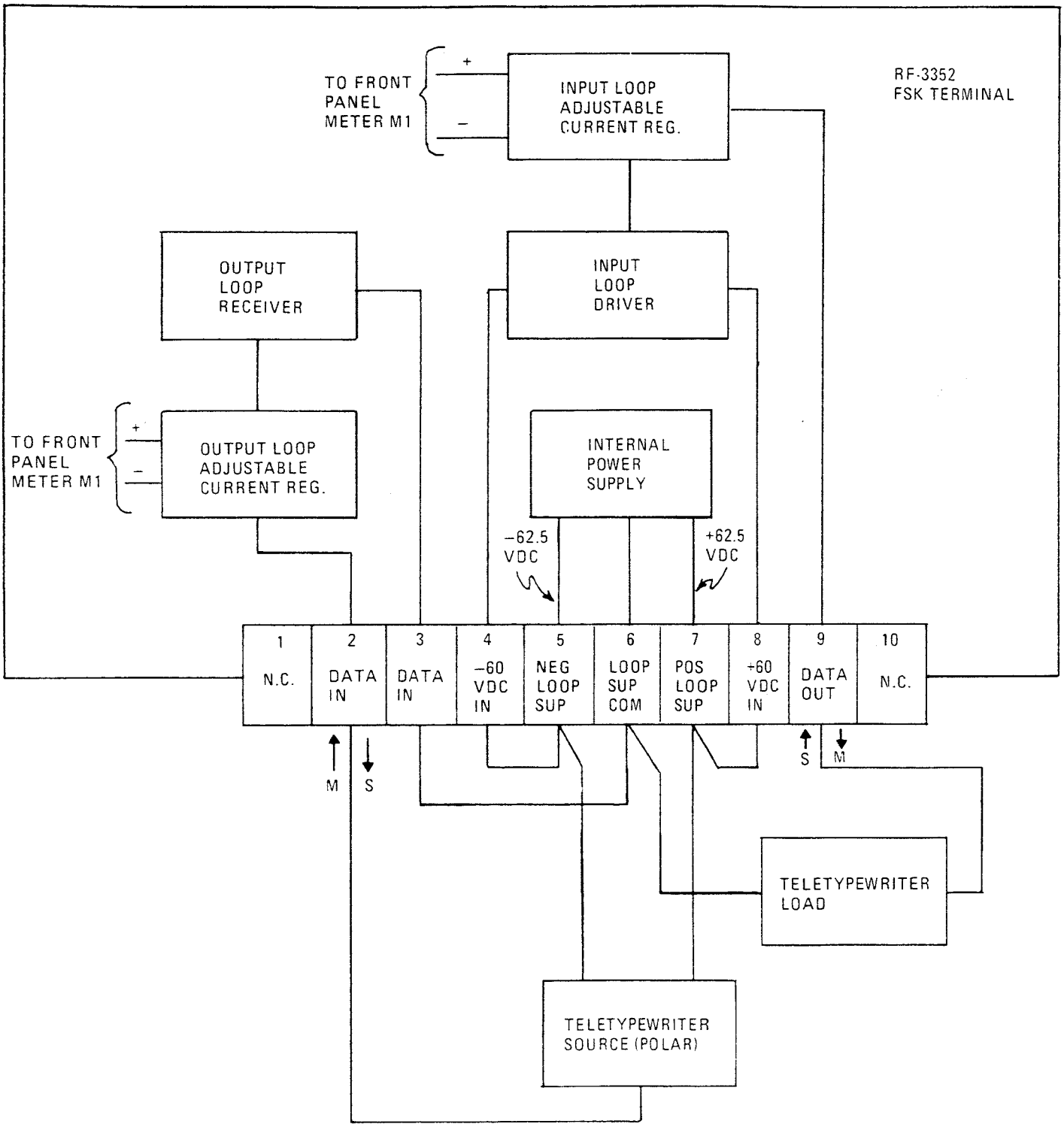


Figure 2-3. RF-3352 FSK Terminal/Teletypewriter Interconnection - Polar Mode - Independent Loops (Full Duplex)

Table 2-1. Accessories Shipped with the RF-3352 FSK Terminal

(Accessory Kit Part No. 6918-0020)

Item No.	Qty.	Part No.	Name
1	1	724-0029	AC Power Cord
2	1	J22-0001-001	RS-232 Connector
3	1	J22-0001-002	Low Level Connector
4	15	E60-0001-001	Solderless Terminals
5	2	K55-0010-003	Connector Clamps
6	1	MS 3106A - 10SL - 35	Auto-Start Connector
7	1	MS 3057 - 4B	Connector Clamp
NOTE: Model RF-3352 FSK Terminal, ordered as Part No. 6918-0010, includes RF-3352 FSK Terminal Part No. 6918-1100, Accessory Kit Part No.6918-0020 and RF-3352 FSK Terminal Instruction Manual Part No. 6918-0100.			

Figure 2-4 shows the RF-3352 FSK Terminal internal interconnection of the unit's assemblies and major components. The identity of assembly connectors and the function of all rear panel connector pins is given.

Examine Input/Output Connector W4J4 in Figure 2-4. Note that there are two sets of audio input and audio output, diversity signal, and diversity gain connections. This scheme allows the connection of two or more equipments to the terminal (this scheme is sometimes referred to as "daisy-chaining"). Provision for a hand key input (W4J4-23) is also provided. An audio strapping capability (the linear combination of two audio signals - one superimposed on the other) is also provided (at W4J4-12 and -25).

2.4.1 PRIMARY POWER SELECTION

Either 115 Vac or 230 Vac may be selected by placing the rear panel Primary Power Selector (1S1, Figure 3-2) in the desired position.

2.4.2 EMERGENCY SHUTDOWN INSTRUCTIONS

In an emergency, place the front panel power ON/OFF Circuit Breaker (1CB1, Figure 3-1) in OFF position. Disconnect primary power.

2.5 INITIAL POSITION OF CONTROLS AND SWITCHES

The following is the suggested initial position of controls and switches, and is to be used as a guide prior to applying power to the terminal. Individual control and switch positions may vary from this guide as individual system requirements dictate. Refer to Figures 3-1 and 3-2 for control and switch locations.

NOTE

If Neutral Mode - Common Loop (Half Duplex) is to be used, refer to the operational discipline in Figure 2-1.

TRANSMIT-KEYLINE CLOSED/AUTO/OPEN Switch A6S1: CLOSED

TRANSMIT-SENSE-NORM/REV/OFF Switch A6S2: NORM

RECEIVE-SENSE-NORM/MARK HOLD/REV Switch A6S3: NORM

TONE SELECTION (Hz)-CENTER FREQUENCY Switch Selection (A7S1): To desired center frequency

TONE SELECTION (Hz)-SHIFT FREQUENCY Switch Section (A7S1): To Desired shift frequency

METER FUNCTION Selector W1S1: AUDIO IN

Rear Panel Primary Power Selector Switch 1S1: To applicable primary power source

Rear Panel LOOPBACK/NORM Switch 1S3/A5S: NORM

2.6 LOOP CURRENT ADJUSTMENTS

The input and output loop currents can be adjusted between 20mA and 60 mA (Polar Mode) or 20 mA and 80 mA (Neutral Mode) in the following manner: Place METER FUNCTION Selector W1S1 in either LOOP IN or LOOP OUT position and adjust either INPUT LOOP ADJUST Control A5R2 or OUTPUT LOOP ADJUST Control A5R1, respectively, to obtain the desired loop current. (Refer to Figures 3-1 and 3-2 for selector and control locations.)

NOTE

To avoid reading errors caused by the averaging effect of the meter movement (for example, Mark/Space data in Neutral Mode), it is recommended that loop currents be adjusted while constant current is flowing (when terminal is in Mark Hold).

2.7 OPERATIONAL ADJUSTMENTS

Certain adjustments that allow the terminal to be operated in accordance with specific user requirements can be accomplished. The following defines the applicable control nomenclature and adjustment characteristics. The location of these controls is shown in Figures 5- through 5- .

a. Receiver Loop NEUTRAL/POLAR Switch A4S1 — Place this switch in the desired position.

b. PSDTR (Pseudo Data Terminal Ready) Switch A4S2 — Allows data to be input at RS-232 levels without going through the RS-232 protocol. Place switch in desired position.

NOTE

The PSDTR Switch will override the current loops. Make sure switch is at the proper position prior to energizing unit.

c. AS OVERRIDE Switch A4S3 — Placing this switch ON causes the Auto-Start Relay to remain closed.

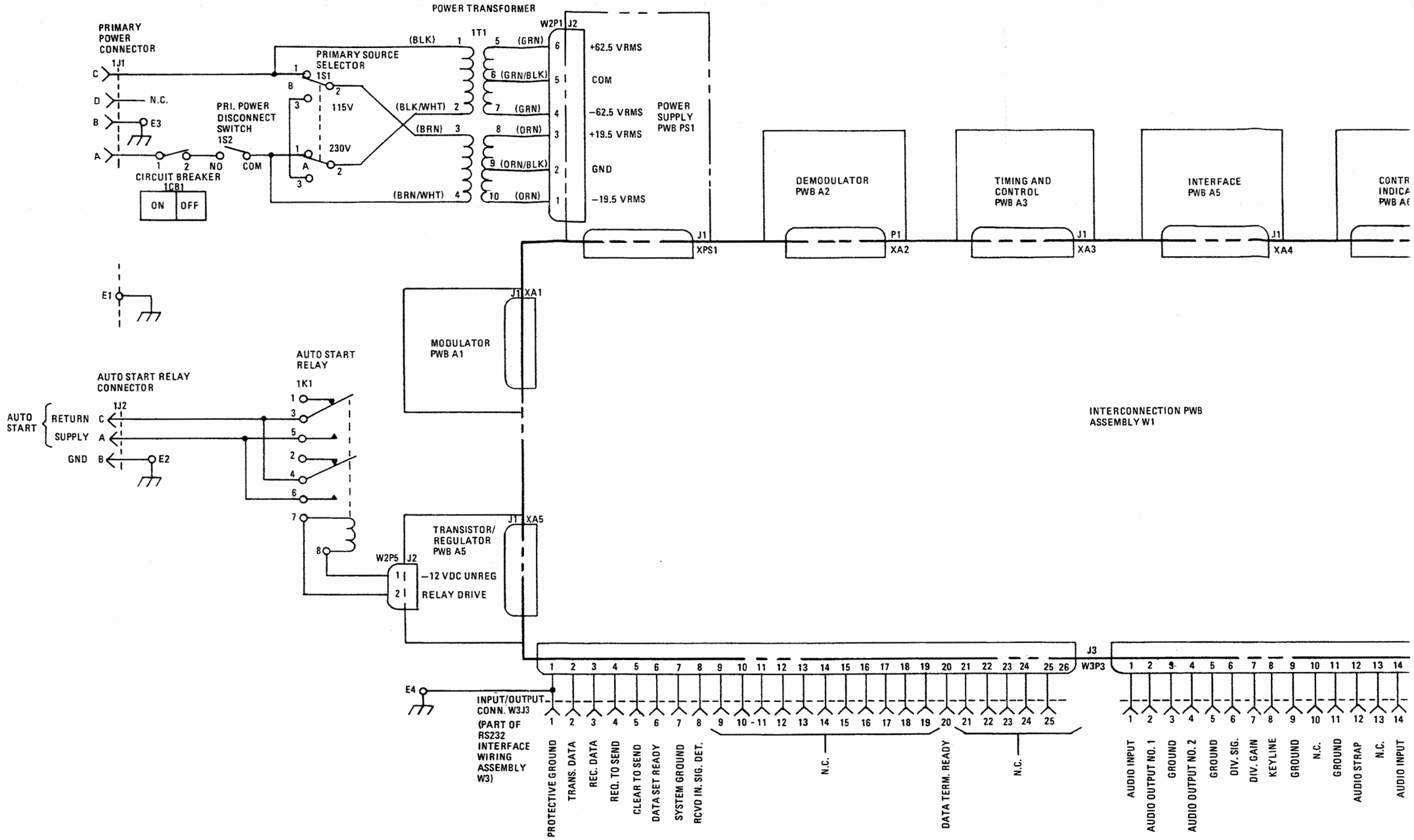
d. IDLE SELECT Switch A1S1 — Allows the terminals output to be a Mark Tone (high or low, depending on the setting of the front panel TRANSMIT-SENSE-NORM/REV Switch A6S2) or no tone.

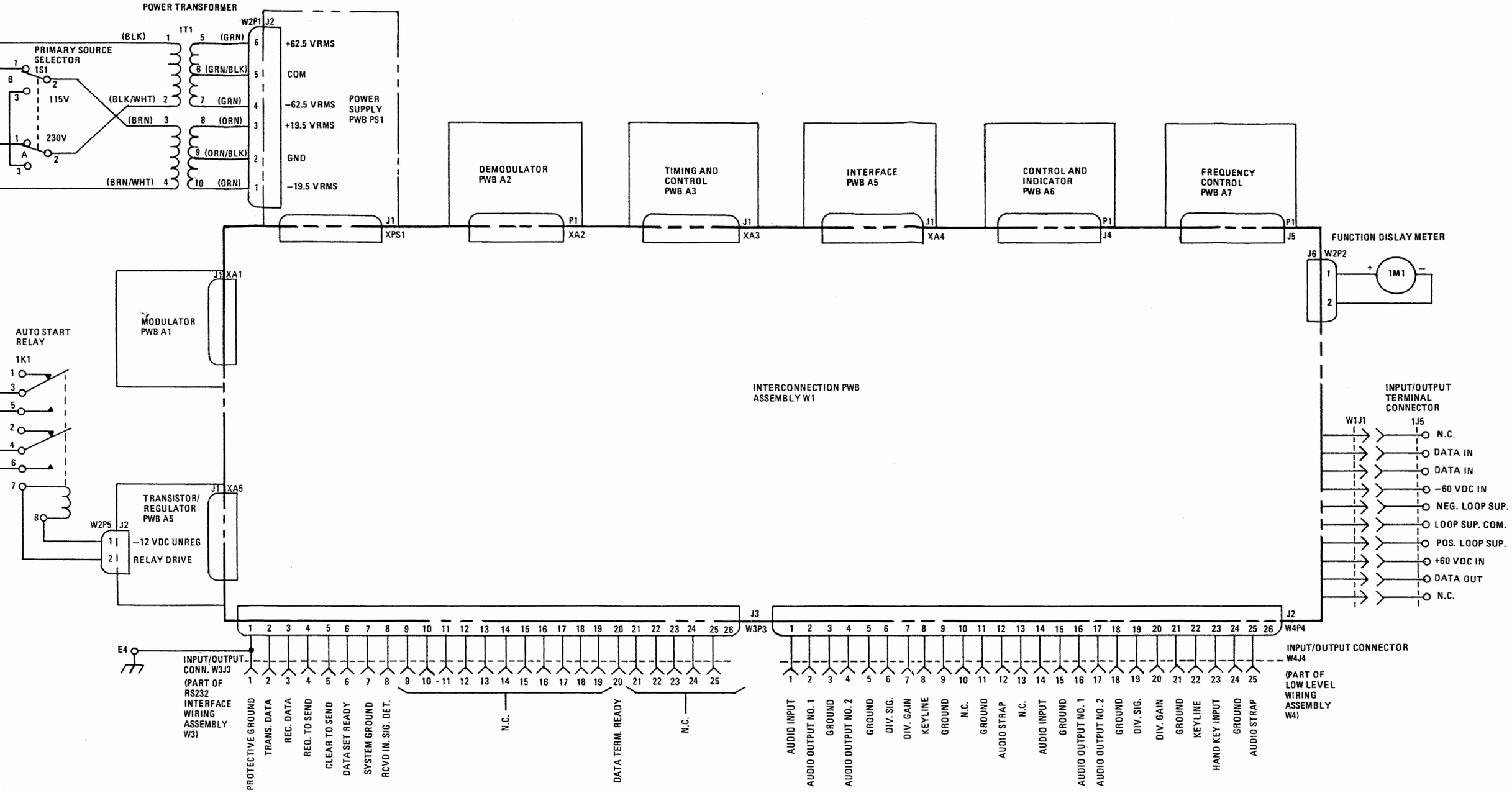
e. TRAF. HOLD TIME Potentiometer A1R30 — Adjustable between 0.4 second and 2.5 seconds following the final data state transmission. It is factory set at 1.0 second.

f. CLEAR TO SEND DELAY Potentiometer A1R32 — Adjustable between 0.1 second and 2.5 seconds. It is factory set at 1.0 second.

2.8 REPACKING AND SHIPPING INSTRUCTIONS

If the terminal or any of its subassemblies are to be shipped or returned to the factory, or shipped elsewhere, standard packing instructions for electronic equipment apply. For example, careful wrapping of electronic parts and assemblies and correct marking of containers and applicable destination instructions and codes are all included in standard packing procedures. Follow the instructions of the nearest responsible authority.


POWER TRANSFORMER
PRIMARY POWER CONNECTOR
1J1
C
D
N.C.
B
E3
A
1 2 NO COM
CIRCUIT BREAKER 1CB1
ON OFF
PRIMARY SOURCE SELECTOR 1S1
PRI. POWER DISCONNECT SWITCH 1S2
115V
230V
1T1
(BLK) 1
(BLK/WHT) 2
(BRN) 3
(BRN/WHT) 4
5 (GRN)
6 (GRN/BLK)
7 (GRN)
8 (ORN)
9 (ORN/BLK)
10 (ORN)
W2P1 J2
+62.5 VRMS
COM
−62.5 VRMS
+19.5 VRMS
GND
−19.5 VRMS
POWER SUPPLY PWB PS1
J1 XPS1
DEMODULATOR PWB A2
P1 XA2
TIMING AND CONTROL PWB A3
J1 XA3
INTERFACE PWB A5
J1 XA4
CONTR INDICA PWB AE
E1
J1 XA1
MODULATOR PWB A1
INTERCONNECTION PWB ASSEMBLY W1
AUTO START RELAY
AUTO START RELAY CONNECTOR
1J2
AUTO START
RETURN C
SUPPLY A
GND B
E2
1K1
TRANSISTOR/ REGULATOR PWB A5
J1 XA5
W2P5 J2
1 −12 VDC UNREG
2 RELAY DRIVE
J3 W3P3
E4
INPUT/OUTPUT CONN. W3J3
(PART OF RS232 INTERFACE WIRING ASSEMBLY W3)
1 PROTECTIVE GROUND
2 TRANS. DATA
3 REC. DATA
4 REQ. TO SEND
5 CLEAR TO SEND
6 DATA SET READY
7 SYSTEM GROUND
8 RCVD IN. SIG. DET.
9 10 11 12 13 14 15 16 17 18 19 N.C.
20 DATA TERM. READY
21 22 23 24 25 N.C.
1 AUDIO INPUT
2 AUDIO OUTPUT NO. 1
3 GROUND
4 AUDIO OUTPUT NO. 2
5 GROUND
6 DIV. SIG.
7 DIV. GAIN
8 KEYLINE
9 GROUND
10 N.C.
11 GROUND
12 AUDIO STRAP
13 N.C.
14 AUDIO INPUT



AUDIO IN 1/14 GRN/BLK
OUT(1) 2/16
OUT(2) 4/17 RED/BLK
KEYLINE 8/22 NO. REV WHT/BLK

Figure 2-4. RF-3352 FSK Terminal Interconnection and Assembly Identification Diagram

SECTION 3

OPERATION

3.1 INTRODUCTION

This section contains or references the information necessary to operate the RF-3352 FSK Terminal.

3.2 FRONT AND REAR PANEL CONNECTOR CONTROL, INDICATOR AND SWITCH LOCATIONS AND FUNCTIONS

Figures 3-1 and 3-2 show the location of all RF-3352 FSK Terminal front and rear panel connectors, controls, indicators and switches. The function of these components is described in Table 3-1.

3.3 OPERATION

The RF-3352 FSK Terminal responds to, and functions in accordance with, signal data applied to it from other system components (such as radio transmitters, receivers, and teletypewriter/teleprinter equipment). The terminal, when interconnected as shown in Figures 2-1 through 2-3, will operate in the manner prescribed. Under normal circumstances, no further adjustment or repositioning of controls will be necessary.

When transmitting or receiving on Upper Sideband (USB), the transmit and receive sensing switches (TRANSMIT-SENSE NORM/REV/OFF Switches A6S2 and RECEIVE-SENSE NORM/MARK HOLD/REV Switch A6S3, respectively) are generally placed in NORM position. When Lower Sideband (LSB) is used, the switches are normally placed in REV position. Intermixing the sensing switch positions may cause a garbled or distorted output at the teletypewriter equipment.

3.4 DETERMINING THE UNKNOWN CENTER AND SHIFT FREQUENCIES

In the event that it is desired to determine unknown center and shift frequencies, the following method can be used.

NOTE

The following procedure assumes that the terminal is connected in the link and operating normally.

a. Refer to Figure 3-1. Place METER FUNCTION Selector W1S1 in AGC position.

b. While slowly rotating the TONE SELECTION (Hz)-CENTER FREQUENCY Switches A7S1, observe and record the lowest (below zero) and highest (above zero) pointer deflections of the Function Display Meter 1M1. (These points will correspond to f_L and f_H, respectively, in subsequent step c.)

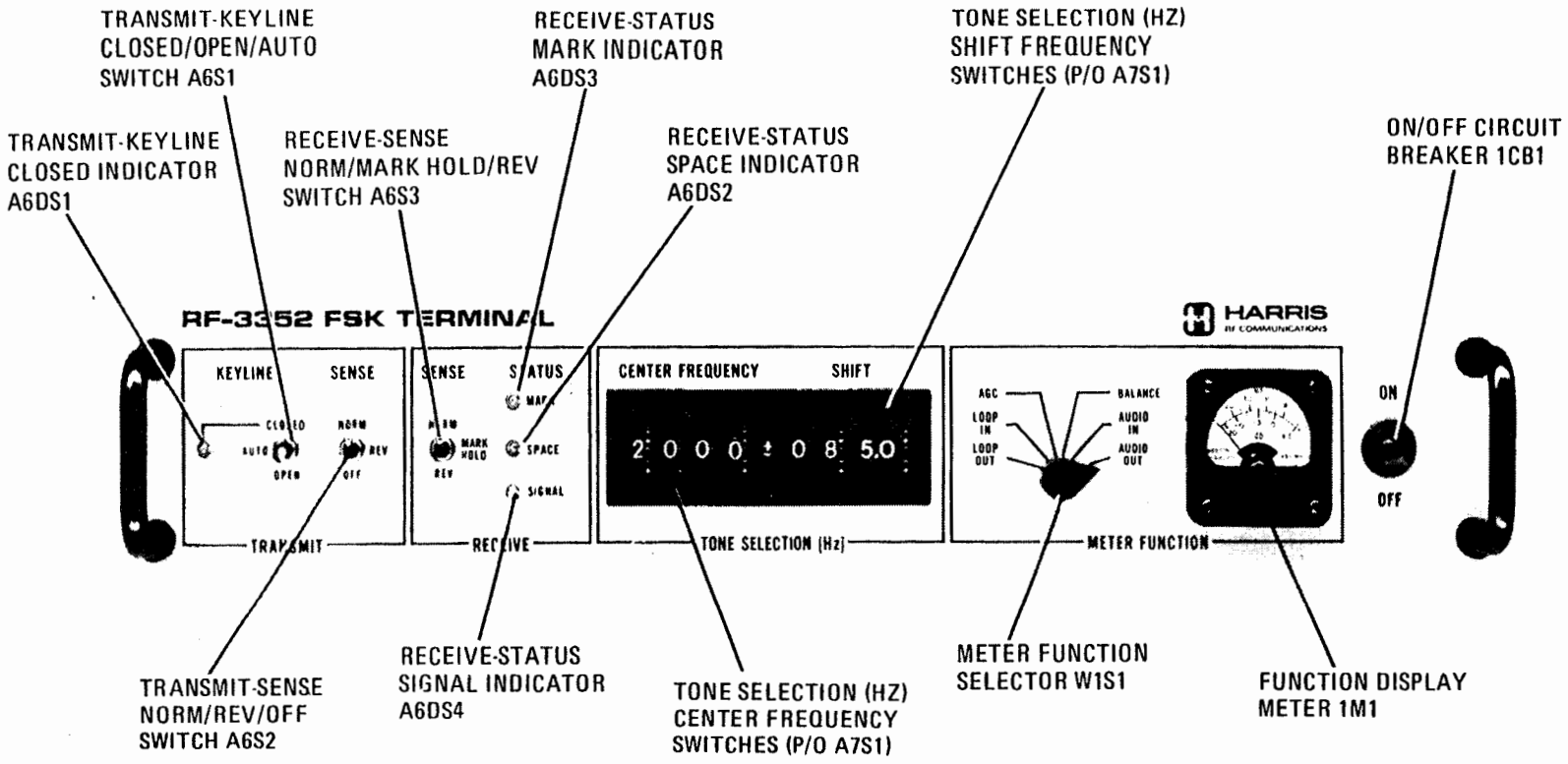


Figure 3-1. RF-3352 FSK Terminal Front Panel Controls, Indicators, and Switches

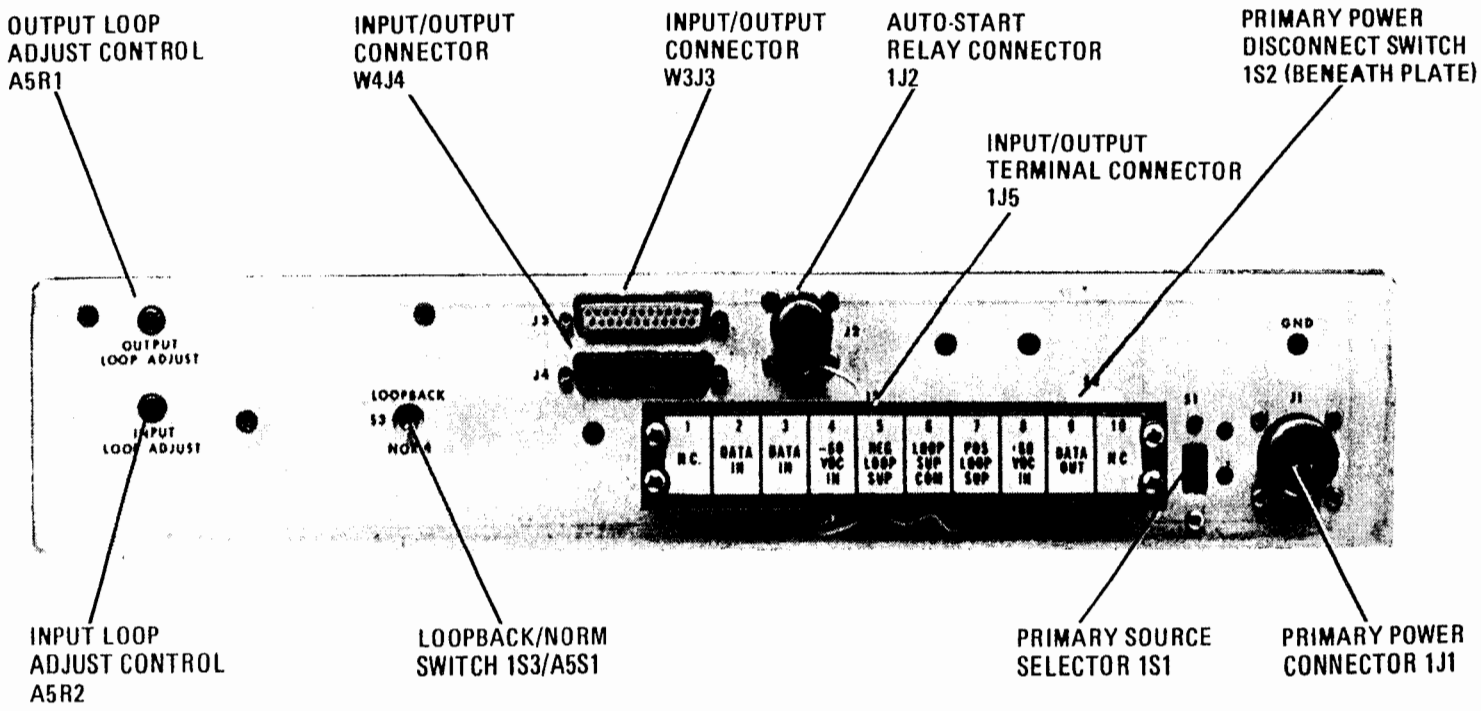


Figure 3-2 RF-3352 FSK Terminal Rear Panel Connectors, Controls, and Switches

Table 3-1. RF-3352 FSK TERMINAL - EXTERNAL CONNECTOR, CONTROL, INDICATOR AND SWITCH FUNCTIONS

(Note: Refer to Figure 3-1 and 3-2 for component locations.)

Name and Reference Designator	Purpose and/or Function
Front Panel:	
TRANSMIT-KEYLINE-CLOSED Indicator A6DS1	Indicates that the system transmitter is operating through the terminal.
TRANSMIT-KEYLINE-CLOSED/ OPEN/AUTO Switch A6S1	Allows closing and opening of the transmit path through the terminal; also allows terminal auto matic response to the transmitted signal.
TRANSMIT-SENSE-NORM/REV/ OFF Switch A6S2	Allows selection of normal or inverted signal transmission; when switch is OFF, allows an audio strapped input to be monitored by the system independent of terminal-generated signals.
RECEIVE-SENSE-NORM/MARK HOLD/REV Switch A6S3	Allows selection of normal or inverted signal reception; also allows terminal to be maintained in a steady Mark Hold state.
RECEIVE-STATUS-MARK Indicator A6DS3	Indicates the presence of a received signal with Mark characteristics.
RECEIVE-STATUS-SPACE Indicator A6DS2	Indicates the presence of a received signal with Space characteristics.
RECEIVE-STATUS-SIGNAL Indicator A6DS4	Indicates the presence and terminal decoding of a received signal.
TONE SELECTION (Hz)-CENTER FREQUENCY Switches A7S1	Allows selection of any center frequency between 270 Hz and 3400 Hz.
TONE SELECTION (Hz)-SHIFT Frequency Switches A7S1	Allows selection of any shift frequency between 0.0 Hz and 597.5 Hz.
METER FUNCTION Selector W1S1:	
LOOP OUT Position	Allows Function Display Meter 1M1 to indicate system output loop current.
LOOP IN Position	Allows Function Display Meter 1M1 to indicate system input loop current.
AGC Position	Allows Function Display Meter 1M1 to indicate the automatic gain control voltage level.

Table 3-1. RF-3352 FSK TERMINAL EXTERNAL CONNECTOR, CONTROL, INDICATOR AND SWITCH FUNCTIONS (Cont.)

(Note: Refer to Figures 3-1 and 3-2 for component locations.)

Name and Reference Designator	Purpose and/or Function
Front Panel (Cont.)	
BALANCE Position	Allows Function Display Meter 1M1 to indicate the amplitude and polarity of the demodulator threshold (reference) signal.
AUDIO IN Position	Allows Function Display Meter 1M1 to indicate the strength of the received audio input signal.
METER FUNCTION Selector W1S1: (cont.)	
AUDIO OUT Position	Allows Function Display Meter 1M1 to indicate the strength of the terminals audio output signal.
Function Display Meter 1M1	Indicates the function selected by METER FUNCTION Selector W1S1. Meter dial indicates 0 to 106 mA and -10dB to +3dB.
ON/OFF Circuit Breaker 1CB1	Allows application of primary power to the terminal.
Rear Panel:	
OUTPUT LOOP ADJUST Control A5R1	Allows adjustment of the output loop current to the desired level.
INPUT LOOP ADJUST Control A5R2	Allows adjustment of the input loop current to the desired level.
LOOPBACK/NORM Switch 1S3/A5S1	Allows evaluation of system components independent of the influence of the radio link.
Input/Output Connectors W3J3 and W4J4; Input/Output Terminal Connector 1J5	Allows terminal functional connections to and from system components.
Auto-start Relay Connector 1J2	Allows system connection to Auto-start Relay 1K1.
Primary Power Selector 1S1	Allows selection of either 115 Vac or 230 Vac primary power.
Primary Power Connector 1J1	Allows connection of primary power source to terminal.

c. Find the unknown center frequency (f_c) and shift frequency f_s) using the method described in the following example:

Example:

f_L (from step b) = 1020 Hz

f_H (from step b) = 1580 Hz

f_c = Unknown Center Frequency

f_s = Unknown Shift Frequency

$$f_c = f_L + \frac{f_h}{2} = \frac{1020\ Hz + 1580\ Hz}{2} = 1300\ Hz$$

$f_s = f_h - f_c = 1580\ Hz - 1300\ Hz = 280\ Hz$

also $f_s = f_c - f_l = 1300\ Hz - 1020\ Hz = 280\ Hz$

d. Set TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1 to 1300 Hz

e. Set TONE SELECTION (Hz) - SHIFT FREQUENCY Switches A7S1 to ± 280 Hz.

3.5 DETERMINING THE UNKNOWN CENTER FREQUENCY WHEN THE SHIFT IS KNOWN

In the event that it is desired to determine an unknown center frequency when the shift frequency is known, the following method can be used.

NOTE

The following procedure assumes that the terminal is connected in the link and operating normally.

a. Refer to Figure 3-1. Place METER FUNCTION Selector W1S1 in AGC position.

b. Set TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1 to the known shift frequency.

c. While slowly routing the TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1, observe the pointer defective on Function Display Meter 1M1. At the first point of maximum pointer defective (either above or below zero), place METER FUNCTION Selector W1S1 in BALANCE position and observe the meter pointer. If the pointer displays an average deflection significantly to the right or left of zero, the frequency indicated by the center frequency switches is incorrect. If the pointer deflection is centered near zero, the set center frequency is the correct center frequency.

3.6 LOOP CURRENT ADJUSTMENT

Refer to paragraph 2.6 for the input and output loop current adjustment procedure.

3.7 EMERGENCY SHUTDOWN INSTRUCTIONS

In an emergency, place the front panel power ON/OFF Circuit Breaker (1CB1, Figure 3-1 in OFF position. Disconnect primary power.

SECTION 4

THEORY OF OPERATION

4.1 INTRODUCTION

The RF-3352 FSK Terminal comprises Modulator Pwb A1, Demodulator Pwb A2, Timing and Control Pwb A3, Interface Pwb A4, Transistor Regulator Pwb A5, Control and Indicator Pwb A6, Frequency Control Board Assembly A7, and Power Supply Pwb PS1. These major assemblies are electrically connected to or interconnected by Interconnection Pwb W1, Chassis and Panel Wiring Assembly W2, RS-232 Interface Wiring Assembly W3, and Low Level Wiring Assembly W4. The individual and interrelated functions of these components are described in this section. Refer to Table 7-2, Page 7-4, for a description of the abbreviations and acronyms used in this section.

4.2 OVERALL TERMINAL AND SUBASSEMBLY FUNCTIONAL DESCRIPTIONS

The RF-3352 FSK Terminal is a modern (modulator/demodulator) device that provides for two-way operation of radio teleprinter equipment over a radio link. The Interface Pwb (A4) accepts incoming data, in either RS-232 or Current Loop format, converts it to internal logic levels, and routes it to the Modulator Pwb (A1). The Modulator Pwb (A1) encodes the data into two FSK audio subcarriers, which are in turn transmitted via radio. The Demodulator Pwb (A2) decodes or converts received FSK audio subcarriers into serial NRZ and, via Interface Pwb (A4), makes the data available to teleprinter equipment in either RS-232 or Current Loop format.

The Timing and Control Pwb (A3) processes the frequency selected by the front panel frequency selector switches (Frequency Control Board Assembly A7) that is used by the phase locked loop synthesizers of the Modulator Pwb (A1). Timing and Control Pwb (A3) also provides the timing reference frequencies that are used by the other components of the terminal.

The Interface Pwb (A4) contains the input loop receiver circuitry (loop to CMOS), output loop drivers (CMOS to loop), RS-232 receiver (RS-232 to CMOS), RS-232 driver (CMOS to RS-232) and auto start relay driver circuitry. The current loop drivers can be operated from either the internal loop supply (Power Supply Pwb PS1) or from independent external loop supplies.

The Transistor/Regulator Pwb (A5) contains components whose functions are related to other assemblies of the terminal, but whose heat sinking requirements require a remote mounting (except for NORM/LOOPBACK Switch A5S1/1S3, which is mounted to the pwb to allow rear panel access).

The Control and Indicator Pwb (A6) contains the transmit, receive and keyline sensing switches and condition status indicators.

The Frequency Control Board Assembly (A7) contains the center and shift frequency tone selector switches.

The Power Supply Pwb (PS1) provides the dc voltages and loop current required for terminal component operation and, if required, external teleprinter equipment.

The Interconnection Pwb (W1) contains the trace wiring and interconnection receptacles that facilitate signal routing and wiring of the terminal's pwb's, and other components.

Wiring Assemblies W2 through W4 facilitate various signal and voltage routings within the terminal, and provide access to various external equipment via rear panel input/output connectors.

4.3 SIGNAL PATH ROUTING FOR VARIOUS OPERATIONAL STATES

Signal path routings for the various operational states of the terminal are shown in Figures 2-1 through 2-3 and described in detail in Paragraph 4.4.4

4.4 MAJOR ASSEMBLY OPERATIONAL ANALYSES

The following subparagraphs describe the operation of each major assembly, their circuits, and their associated components in detail. Reference to applicable tables, functional diagrams, and to the schematic diagrams of Section 7 is made throughout.

4.4.1 MODULATOR PWB ASSEMBLY A1 OPERATION DESCRIPTION

4.4.1.1 Overall Description

Refer to figure 4-1. Frequency Control Words C-S and C+S (corresponding to the Low and High FSK Tones, respectively) and a 500 Hz square wave input (from Timing and Control Pwb Assembly A3) are applied to two identical Phase-Locked Loop Synthesizers. The synthesizer outputs N (500) are applied to a two-input/one-output Multiplexer. The Multiplexer, controlled by the Control Logic Circuitry, selects one of the synthesizer outputs for subsequent frequency division and conversion to a sinusoid waveform.

The Multiplexer output is applied to a divide-by-200 counter, consisting of the divide-by-10 BCD Counter and divide-by-20 Johnson Counter shown. The counter output, 10 signal lines, is digital-to-analog converted into a 20-step sine wave approximation N (2.5). The sine wave output is level-adjusted, filtered and transformer-coupled, providing two identical audio outputs. The filtered audio is also ac-to-dc converted (rectified) to facilitate terminal front panel meter display and monitoring.

An audio strapping feature is also provided. This allows the linear combination of two or more audio signals.

Various operator-controlled and externally-generated signals are combined in the Control Logic Circuitry, allowing operation of the Modulator in a prescribed manner. (The Modulator is capable of operation in accordance with Specification RS-232C requirements, as well as with standard direct teletypewriter interconnections). Automatic keyline closure upon detection of transmitted data, via the Traffic Detection Circuitry, is operator selectable.

In the Normal Mode of terminal operation, the input transmitted data (Tx Data Input) controls the Multiplexer such that a Low tone output corresponds to a Mark level, and a High tone output corresponds to a Space level. In Reverse mode, these relationships are reversed (Low tone corresponds to Space level, High tone corresponds to Mark level). When no transmitted data is present (transmitter is idle), a constant Mark tone will be present. If the operator chooses, the tone may be eliminated.

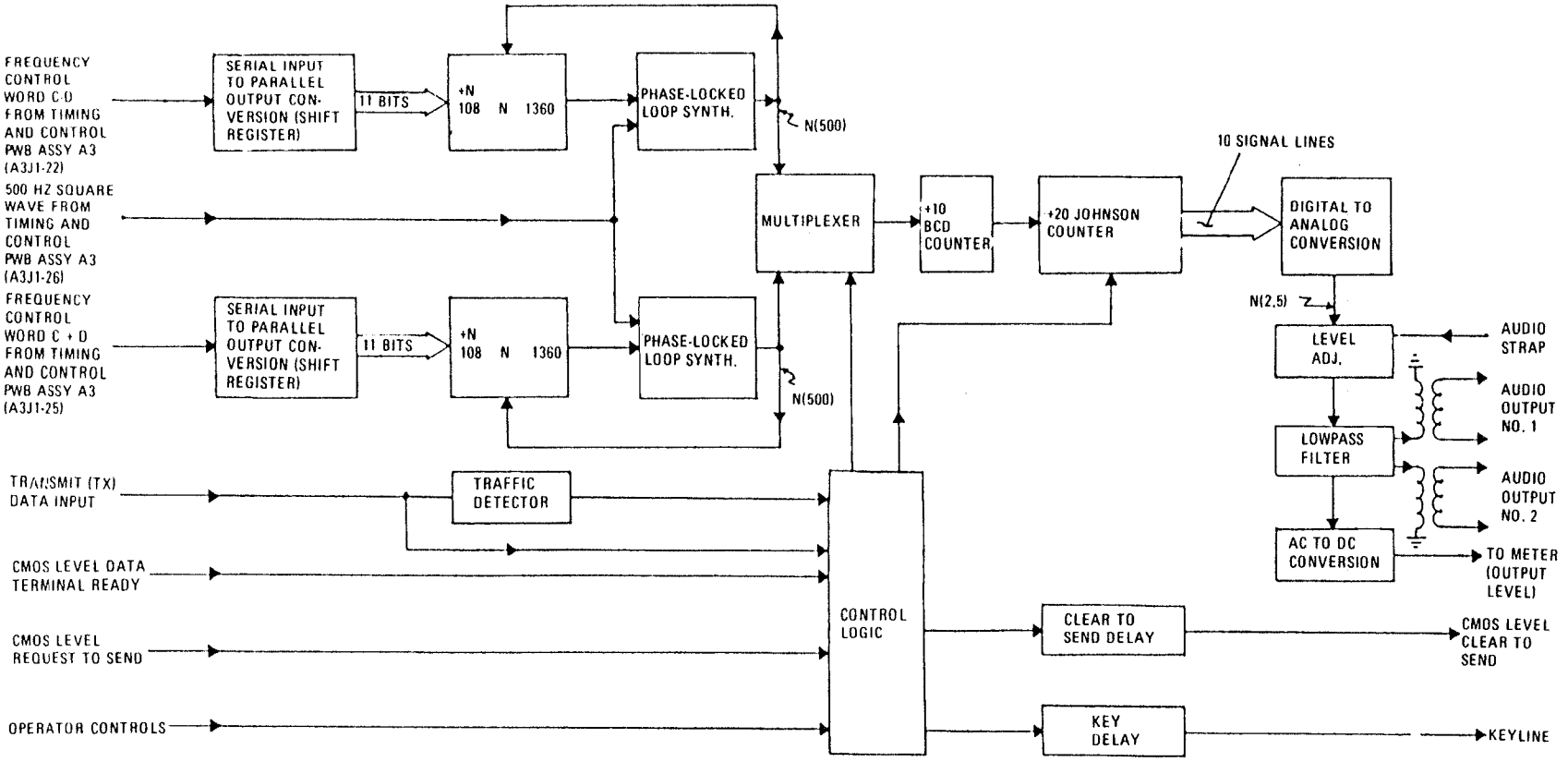


Figure 4-1. Modulator Pwb Assembly A1 Functional Block Diagram

4.4.1.2 Detailed Circuit Description

NOTE

In the following paragraph, parenthetical references refer to the functionally-identical components of the duplicate circuit, unless indicated otherwise.

The Modulator tone-generating circuits consist of two identical phase-locked frequency synthesizers. Refer to Figure 7-2. These synthesizers comprise phase-locked loop U5 (U3), its associated components, and a presettable down counter. The down counter consists of counters U10 and U15 (U21 and U26), a four-input NOR gate U9-9-10-11-12-13 (U9-2-3-4-5-1), a D-type flip-flop U4-8-9-10-11-12-13 (U4-1-2-3-4-5-6), and an inverter U2-5-6 (U2-1-2).

4.4.1.2.1 Phase-locked Loop Operation

Refer to Figure 7-2. Phase locked loop (U5) (U3) tries to set its input frequency (Pin 4) such that its input frequency (Pin 3) will equal the 500 Hz reference frequency (Pin 14). If the output frequency is divided by an integer (N) to produce the input frequency, and if the input frequency is also equal to the 500 Hz reference frequency applied, the output frequency will equal the reference frequency multiplied by N. Stated symbolically:

$$\text{If: } f_{\text{INPUT (Pin 3)}} = \frac{f_{\text{OUTPUT (Pin 4)}}}{N} = f_{\text{REFERENCE (Pin 14)}}$$

$$\text{Then: } f_{\text{OUTPUT}} = N \times f_{\text{REFERENCE}}$$

N, the required multiplication factor, is provided by a frequency divider (counter) whose input is the square wave at the output of the loop (Pin 4), and whose output frequency equals the reference frequency.

4.4.1.2.2 Divide-by-N Counter Operation

Refer to Figure 7-2. Integrated circuit components U10 and U15 (U21 and U26) comprise a cascaded down counter containing a maximum of 4096 states. Its operation is described in the following subparagraphs.

For reference purposes, assume that the counter has just been clocked into State No. 1 at time t = 0. State No. 1 is recognized by NOR Gate U9-9-10-11-12-13 (U9-2-3-4-5-1), which produces a High at the D input of Flip-flop U4 (U4-9 (U4-5). At time T/2 (T being the period of the square wave clock input), U4's Q output U4-13 (U4-1) goes High, forcing the counter into State M. State M is the decimal equivalent of the binary number applied to the counter's Preset (J) inputs.

At the time that the counter is forced into State M (time T/2), Flip-flop U4's D input U4-9 (U4-5) goes Low. Its Q input U4-13 (U4-1) goes Low at time 3T/2. With the forced loading signal now removed, the counter is free to be clocked to State M-1 when timeT2 occurs. At time 3T, the counter will change to State M-2, etc.

In general, the counter state changes to State M - r at time (r + 1)T. Therefore, the counter changes to State No. 1, which is equal to M - (M - 1) at time MT. By making M equal to N, a Divide-by-N counter (modulo) results.

4.4.1.2.3 Binary Number Application to Counter/Latch Operation

Refer to Figure 7-2. The binary numbers that are used to set the counter's division ratio are supplied in a serial bit stream that originates in Timing and Control Pwb A3. In the Modulator, this serial bit stream is applied to a serial input/parallel output shift register U23 and U17 (U23 and U28). The bit stream is shifted into the register by a 31.25 Hz clock. Approximately once each second, when valid data is present at the shift register's parallel outputs, a Latch Pulse is applied to the Clock inputs of Hex D Flip-flops U11 and U16, that is, at U11-9 (U22-9) and U16-9 (U27-9). Thus, the binary number is stored and applied to the Preset (J) inputs of the counter.

NOTE

The only time at which C + S or C-S input data is valid is during the half clock cycle occurring immediately before and after the Latch Command. Data either side of this time frame is invalid.

4.4.1.2.4 Synthesizer Output Routing, Divide-By-10 Counter, Divide-By-20 Johnson Counter and Audio Conditioning

The outputs of the two synthesizers are individually selected by the Transmit Data, through the action of NAND Gate U1 (U1-4-5-6; 8-9-10; 11-12-13) and Inverter U2 (U2-3-4). The output is applied to Divide-by-10 Counter U29.

The output of Divide-by-10 Counter U29 is applied to a Divide-by-20 Johnson Counter. This counter consists of Shift Register U25, Flip-flops U24 and U14 (U-14-8-9-10-11-12-13) and NOR Gate U18. Each of the counter's ten output ports supply a square wave at the fundamental tone frequency. Each square wave is shifted by 18° (U18-1-2-3; 4-5-6; -8-9-10) relative to the signal appearing at the adjacent ports.

The current applied to the summing junction of Op Amp U31 (U31-2) is sinusoidally weighted by the resistances of Resistor Pack U30, forming the 20-step sine wave approximation of the desired tone output generated at the output of Op Amp U31 (U31-1).

NOTE

The first harmonic that is theoretically present in this waveform is the 19th harmonic, and is at a level of 25.6dB below the fundamental frequency.

The output of Op Amp U31 (U31-1) is capacitively coupled to Op Amp U31-6-5-7, filtered by a 5-pole bandpass filter (U32-2-3-1 and U21-6-5-7 and their associated components), and applied to buffers (U32-9-10-8 and U32-12-13-14 and their associated components), which drive Transformers T1 and T2. The transformers provide 600 ohm output impedance audio output at J1-6 and -7 (Transformer T1) and J1-10 and -11 (Transformer T2).

Op Amps U31-9-10-8 and U31-12-13-14 rectify the audio output for application to front panel Function Display Panel Meter 1M1.

AUDIO OUT ADJ. Pot. R18 adjusts the audio output level over the specified -30dBm to 0dBm (600 ohms) range. It is factory-set at 0 dBm. AUDIO LEVEL METER CAL. Pot. R23 Adjusts the corresponding amount of front panel Function Display Meter 1M1 pointer deflection, and is factory set to read 0dB at a 0 dBm level.

4.4.1.2.5 Traffic Detector Circuitry

The Traffic Detector Circuitry comprises Flip-flops U14 (U14-5-3-1-2) and U19 (U19-5-3-1-2), NOR Gate U12 NOR Gate U12 (U12-8-9-10), Exclusive OR Gate U8 (U8-8-9-10) and Retriggerable Monostable U20 (U20-4-5-6-7). Each time the Transmit Data (J1-39) makes a level transition, Flip-flop U19 applies a 7.8 usec trigger pulse to Monostable U20. This causes its Q output to go High. If no more transitions occur (as determined by the R-C time constant of components C15, R29 and R30) the Q output will return to its Low state. If more transitions do occur while the Q output is still High, it will remain High for one time period after the last previous transition. The time period is adjustable from 2.5 to 0.4 second by TRAF. HOLD TIME Pot. R30. The pot. has been factory-set at 1.0 second.

4.4.1.2.6 Combinational Logic Circuitry

The Combinational Logic Circuitry allows either RS-232C Protocol operation or Data Only operation (typically supplied from Teletypewriter Unit). The circuitry also accepts various other operator-originated mode selections. Table 4-1 summarizes the operations of this circuitry.

Referring to Table 4-1, note that the Traffic Detector does not operate under RS-232C Protocol. Also note that, depending on the position of IDLE SELECT Switch S1, the audio output will be either the Mark Tone or zero when no transmit data is present.

4.4.1.2.7 Clear-to-Send Delay Function

When the Terminal is operating in accordance with RS-232C Protocol, a Clear-to-Send Delay is provided by Retriggerable Monostable U20 (U20-4-5-6-7). This delay is adjustable, via CLEAR-TO-SEND DELAY Pot. R32, from 0.1 to 2.5 seconds. This delay is factory-set at 1.0 second.

4.4.1.2.8 Keyline Closure Function

Refer to Figure 7-2. Keyline Closure is provided by DPST Relay K1. One set of contacts control front panel TRANSMIT-KEYLINE CLOSED Indicator A6DS6.

Table 4-1. MODULATOR PWB A1 CONTROL LOGIC TRUTH TABLE DATA

Conditions							Effects	
TRANSMIT - KEYLINE CLOSED/OPEN/AUTO Switch A6S1 (Keyline Control Position	TRANSMIT - SENSE NORM/REV/OFF Switch A6S2 (Output Control Position	Idle Select SwitchA1S1 Status	Data Terminal Ready	Req. To Send	Transmit (TX) Data	Clear To Send	Keyline Status	Audio Output Status
Open	Off	X	X	X	X	Low	Open	NTO
Auto	Off	X	X	X	X	Low	Open	NTO
Closed	Off	X	X	X	X	Low	Closed	NTO
Open or Auto	Norm. or Rev.	ITOM	Low	X	INA	Low	Open	LT (Norm.), HT (Rev.)
Closed	Norm. or Rev.	ITOM	Low	X	INA	Low	Closed	LT (Norm.), HT (Rev.)
Open or Auto	Norm or Rev.	$\overline{\text{ITOM}}$	Low	X	INA	Low	Open	NTO
Closed	Norm. or Rev.	$\overline{\text{ITOM}}$	Low	X	INA	Low	Closed	NTO
Open	Norm. or Rev.	X	Low	X	A	Low	Open	MLT/SHT (Norm.), SLT/MHT (Rev.)
Auto or Closed	Norm. or Rev.	X	Low	X	A	Low	Closed	MLT/SHT (Norm.), SLT/MHT (Rev.)
Open or Auto	Norm. or Rev.	ITOM	High	Low	X	Low	Open	LT (Norm.), HT (Rev.)
Closed	Norm. or Rev.	ITOM	High	Low	X	Low	Closed	LT (Norm.), HT (Rev.)
Open or Auto	Norm. or Rev.	$\overline{\text{ITOM}}$	High	Low	X	Low	Open	NTO
Closed	Norm. or Rev.	$\overline{\text{ITOM}}$	High	Low	X	Low	Closed	NTO
Open	Norm. or Rev.	ITOM	High	High	X	Low	Open	LT (Norm.), HT (Rev.)
Open	Norm. or Rev.	$\overline{\text{ITOM}}$	High	High	X	Low	Open	NTO
Auto or Closed	Norm. or Rev.	X	High	High	A	High	Closed	MLT/SHT (Norm.), SLT/MHT (Rev.)
⚠1 Auto or Closed	Norm. or Rev.	X	High	High	X	Low	Open	LT (Norm.), HT (Rev.)

LIST OF ABBREVIATIONS/ACRONYMS USED IN TABLE 4-A:

A = Active
HT = High Tone
INA = Inactive
ITOM = Idle Tone Output (Mark Frequency)
$\overline{\text{ITOM}}$ = No Idle Tone Output
LT = Low Tone
MLT/SHT = Mark is being carried on Low Tone/Space is being carried on High Tone
NTO = No (audio output) Tone Output
SLT/MHT = Space is being carried on Low Tone/Mark is being carried on High Tone
X = No effect on Audio Output Status

⚠1 This condition corresponds to the time between Request to Send and the Clear to Send response.

4.4.2 Demodulator Pwb Assembly A2 Operation Description

Subsequent paragraphs 4.4.2.1 through 4.4.2.6 and Figure 4-2 describe the overall operation of the major demodulator circuits at functional block diagram level. A detailed theoretical analysis of peculiar circuitry follows in paragraphs 4.4.2.7 through 4.4.2.18.

4.4.2.1 Input Circuitry Operation

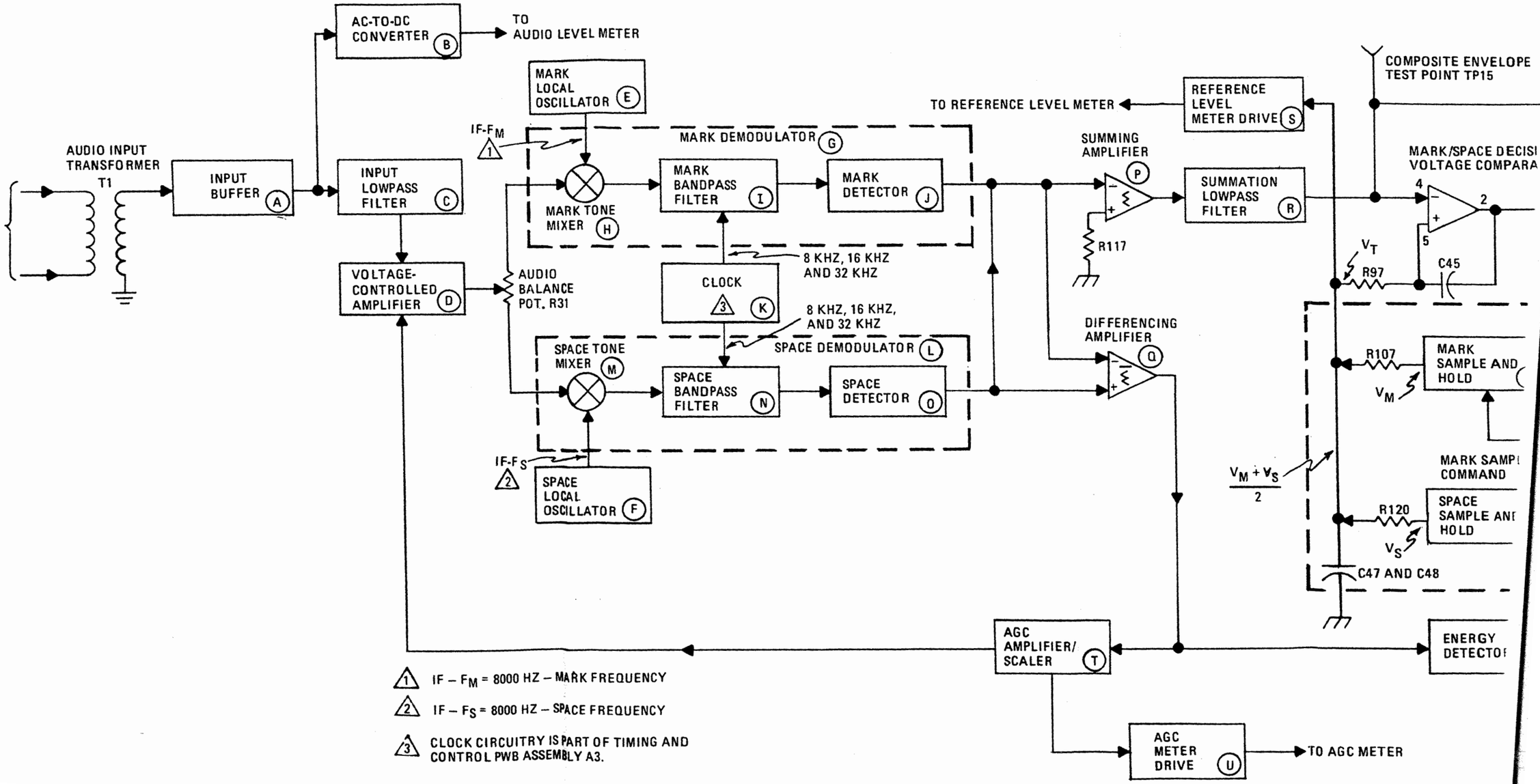
Refer to Figure 4-2. The FSK audio input is coupled through Audio Input Transformer T1 to an impedance-matching Input Buffer A. The buffer's dc output signal is routed to Converter B. The converter's dc output signal is routed to an audio output meter (selected function at the front panel-not shown) which indicates the signal strength of the received input signal.

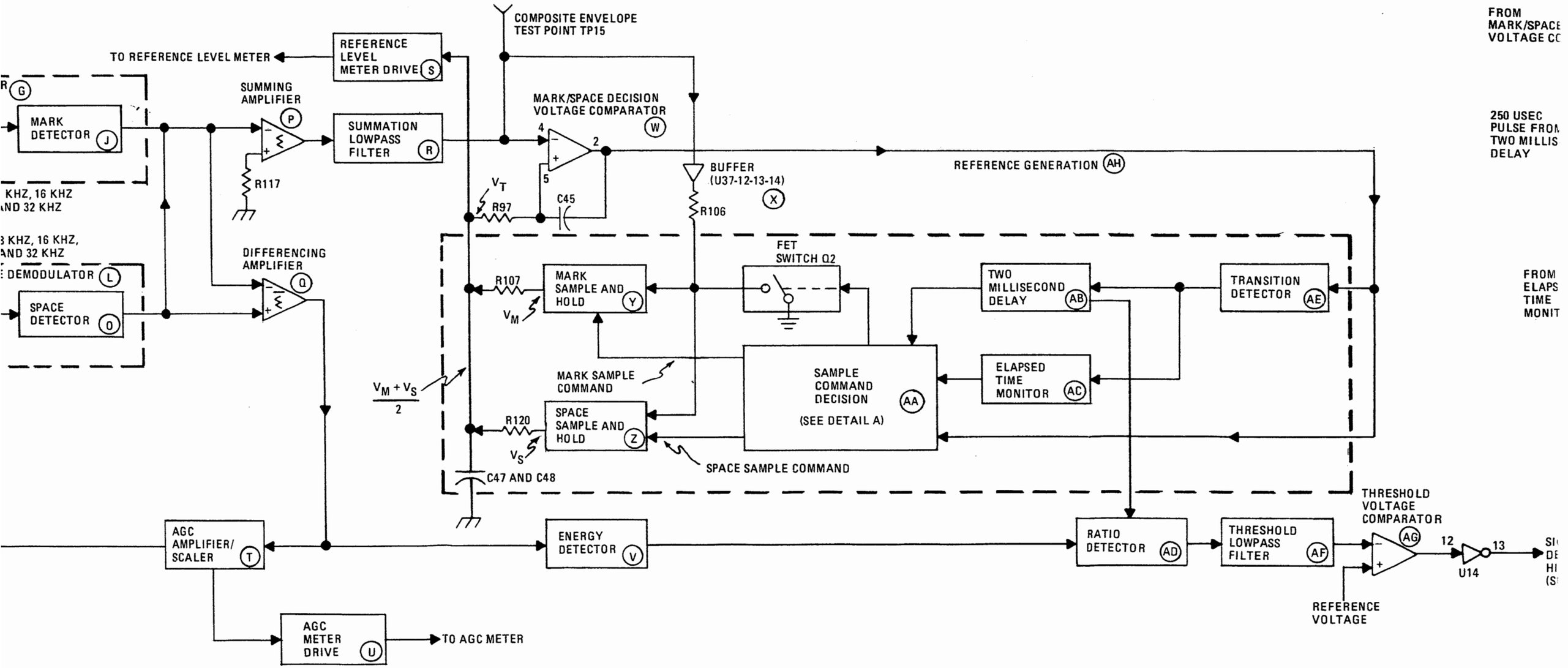
The output of Input Buffer A is also fed to Input Lowpass Filter C, which passes only those signals in the frequency range of the anticipated Mark and Space Tone signals (that is 270 Hz to 3400 Hz).

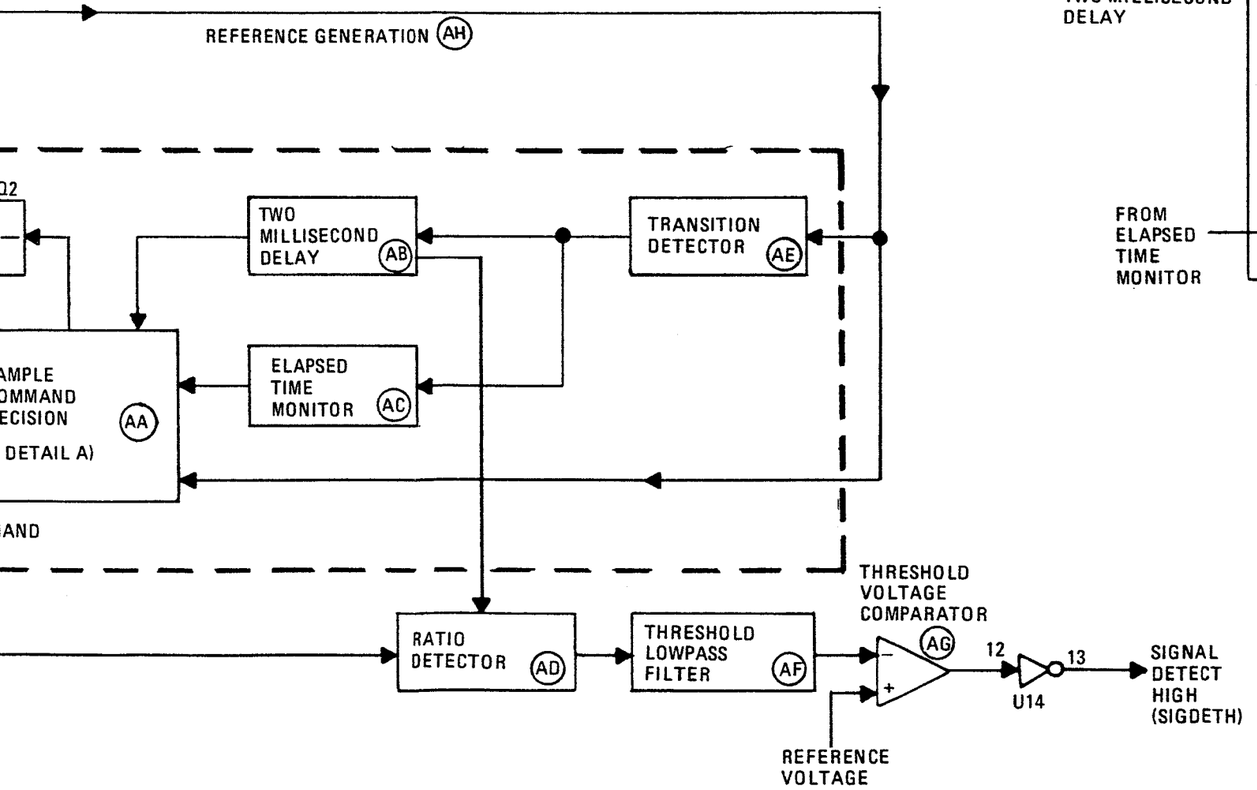
4.4.2.2 Voltage-Controlled Amplifier/Attenuator, Local Oscillator, and Demodulator Circuitry Operation

The output of the Input Lowpass Filter is presented to Voltage Controlled Amplifier/Attenuator D, which is suitably controlled by means of a feedback loop to provide a relatively constant amplitude input signal to Mark Demodulator G and Space Demodulator L. The amplifier's output signal is applied to the demodulators by means of Audio Balance Pot. R31. The potentiometer has been adjusted so that the input signals applied to each demodulator has approximately the same amplitude.

Each demodulator contains a mixer (Mark Tone Mixer H/Space Tone Mixer M) which receives the output signal from the Voltage-Controlled Amplifier/Attenuator D after it has been amplitude-adjusted by Audio Balance Pot. R31. The input signal to each demodulator is combined with a preselected reference signal applied to its mixer from Mark Local Oscillator E and Space Local Oscillator F.


AUDIO INPUT TRANSFORMER T1
INPUT BUFFER A
AC-TO-DC CONVERTER B
TO AUDIO LEVEL METER
INPUT LOWPASS FILTER C
VOLTAGE-CONTROLLED AMPLIFIER D
AUDIO BALANCE POT. R31
MARK LOCAL OSCILLATOR E
IF-FM 1
MARK DEMODULATOR G
MARK TONE MIXER H
MARK BANDPASS FILTER I
MARK DETECTOR J
8 KHZ, 16 KHZ AND 32 KHZ
CLOCK 3 K
8 KHZ, 16 KHZ, AND 32 KHZ
SPACE TONE MIXER M
SPACE BANDPASS FILTER N
SPACE DETECTOR O
SPACE DEMODULATOR L
IF-FS 2
SPACE LOCAL OSCILLATOR F
TO REFERENCE LEVEL METER
REFERENCE LEVEL METER DRIVE S
SUMMING AMPLIFIER P
R117
SUMMATION LOWPASS FILTER R
DIFFERENCING AMPLIFIER Q
COMPOSITE ENVELOPE TEST POINT TP15
MARK/SPACE DECISI VOLTAGE COMPARA
VT
R97
C45
R107
MARK SAMPLE AND HOLD
VM
MARK SAMPI COMMAND
VM + VS / 2
R120
SPACE SAMPLE AN HOLD
VS
C47 AND C48
AGC AMPLIFIER/ SCALER T
ENERGY DETECTO
AGC METER DRIVE U
TO AGC METER
1 IF – FM = 8000 HZ – MARK FREQUENCY
2 IF – FS = 8000 HZ – SPACE FREQUENCY
3 CLOCK CIRCUITRY IS PART OF TIMING AND CONTROL PWB ASSEMBLY A3.


COMPOSITE ENVELOPE
TEST POINT TP15
TO REFERENCE LEVEL METER
REFERENCE
LEVEL
METER DRIVE
S
SUMMING
AMPLIFIER
P
MARK/SPACE DECISION
VOLTAGE COMPARATOR
W
MARK
DETECTOR
J
SUMMATION
LOWPASS
FILTER
R
R117
V_T
R97
C45
BUFFER
(U37-12-13-14)
X
R106
REFERENCE GENERATION
AH
FET
SWITCH Q2
R107
MARK
SAMPLE AND
HOLD
Y
V_M
TWO
MILLISECOND
DELAY
AB
TRANSITION
DETECTOR
AE
DIFFERENCING
AMPLIFIER
Q
SPACE
DETECTOR
O
MARK SAMPLE
COMMAND
SAMPLE
COMMAND
DECISION
AA
(SEE DETAIL A)
ELAPSED
TIME
MONITOR
AC
$\frac{V_M + V_S}{2}$
R120
SPACE
SAMPLE AND
HOLD
Z
V_S
SPACE SAMPLE COMMAND
C47 AND C48
AGC
AMPLIFIER/
SCALER
T
ENERGY
DETECTOR
V
RATIO
DETECTOR
AD
THRESHOLD
LOWPASS
FILTER
AF
THRESHOLD
VOLTAGE
COMPARATOR
AG
12
13
U14
REFERENCE
VOLTAGE
AGC
METER
DRIVE
U
TO AGC METER
FROM
MARK/SPACE
VOLTAGE CO
250 USEC
PULSE FROM
TWO MILLIS
DELAY
FROM
ELAPS
TIME
MONIT



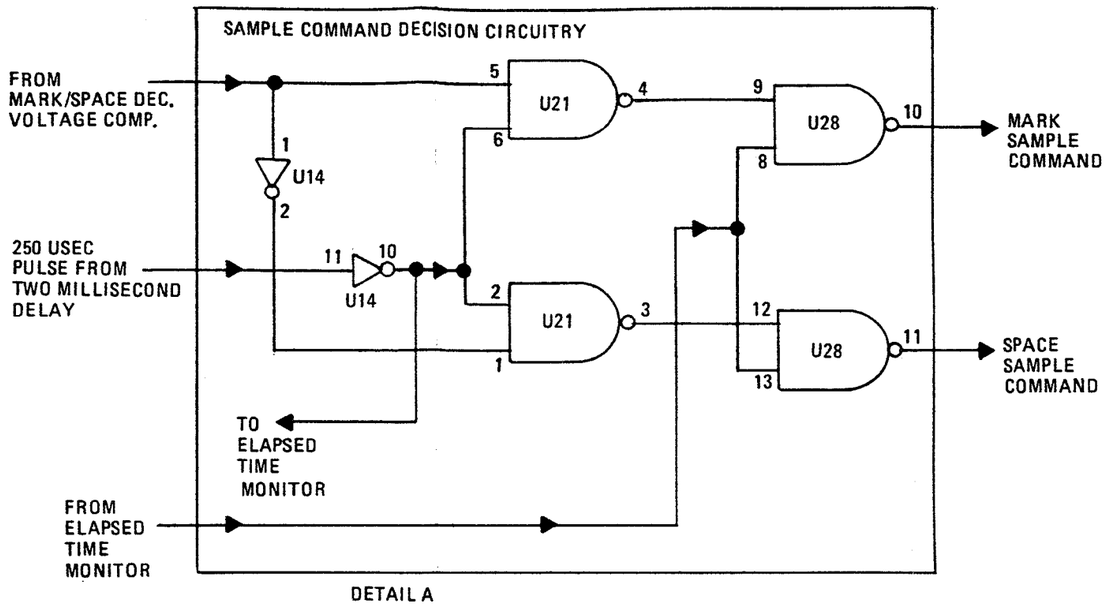


Figure 4-2. Demodulator PWB Assembly A2 Functional Block Diagram

NOTE

The reference signal to each mixer has a frequency equal to the frequency of the tone signal to which the demodulator is responsive. Thus, as noted on Figure 4-2, the reference signal for Mark Tone Mixer H is IF-F_M (where F_M equals the frequency of the Mark tone signal) and the reference frequency for Space Tone Mixer M is IF-F_S equals the fre quency of the space tone signal). Thus, the Mark Tone Mixer H will produce an output signal at the intermediate frequency when a Mark Tone is received, and Space Tone Mixer M will produce an output signal at the intermediate frequency when a Space Tone Signal is received.

The output signals of the Mark Tone Mixer H and Space Tone Mixer M are fed to Mark and Space Bandpass Filters I and N, respectively. As the mixers produce an output signal at the intermediate frequency when either a Mark or a Space Tone is received, the bandpass filters are essentially identical, having a center frequency equal to the intermediate frequency and a relatively narrow bandwidth. The bandpass filters are periodically actuated by Clock K, which is synchronized to the intermediate frequency of 8000 Hz.

When a signal at the intermediate frequency is presented to either one of the bandpass filters by its associated mixer, the filter will produce an output signal having a relatively high amplitude level. The filter output signal is presented to its respective detector (Mark Detector J or Space Detector O). The detectors determine when a high level signal is produced by their associated bandpass filters, and provide an output indicative of this fact.

Although the Mark Detector J and Space Detector O circuits are essentially identical, their corresponding diodes (CR5 and CR6 - Mark Detector, CR2 and CR3 - Space Detector - see Figure 7-3) are reversed. Mark Detector J produces an envelope signal that is negative with respect to ground, while Space Detector O produces an envelope signal which is positive with respect to ground.

4.4.2.3 Summing and Differencing Amplifier Circuitry Operation

The outputs of both the Mark Detector J and Space Detector O are summed at the inverting (negative) input of Summing Amplifier P, thus forming the composite envelope signal. This signal goes positive when a Mark Tone is present and negative when a Space Tone is present.

The negative-going Mark Detector J output is connected to the inverting (negative) input of Differencing Amplifier Q, and the positive-going Space Detector O output is connected to its non-inverting (positive) input. Thus, the output of the amplifier is at a relatively constand positive level. The amplitude of this output is indicative of the energy level of the received audio input signal.

The output signal of Differencing Amplifier Q is routed to the AGC Amplifier/Scaler circuit T. This circuit compares the energy level of Differencing Amplifier Q's output with a predetermined reference value. An output signal indicative of the results of this comparison is fed to the control input of Voltage-Controlled Amplifier/Attenuator D, to automatically adjust the amplitude of the input signal applied to Mark Demodulator G and Space Demodulator L. The output of AGC Amplifier/Scaler T is also fed to the AGC Meter Drive Circuit U, whose output is routed to an AGC meter (selected function at the front panel - not shown) that indicates the automatic gain control voltage level.

4.4.2.4 Mark/Space Decision Voltage Comparator Circuitry Operation

The composite envelope signal output of Summing Amplifier P is passed through Summation Lowpass Filter R, which suppresses high frequency noise. The filter output is fed to the inverting (negative) input of Mark/Space Decision Voltage Comparator W. A threshold signal is applied to the non-inverting (positive) terminal of the comparator from Reference Generation Circuit AH. The comparator compares the amplitude of the composite envelope signal with the threshold signal to determine whether a Mark or Space Tone signal has been received or detected. The comparator produces a binary, serial, synchronized data signal indicative of the information contained in the received FSK audio signal.

4.4.2.5 Reference Generator Circuitry Operation

The output signal from Mark/Space Decision Voltage Comparator W is fed to Transition Detector AE, which detects transitions in the output signal between the two binary levels, and, via the Two Millisecond Delay timer AB, provides control and timing pulses to the Sample Command Decision circuit AA. The 250 microsecond pulse output of Two Millisecond Delay AB is processed in the Sample Command Decision circuit AA to produce either a Mark or a Space Sample Command signal. The other output of Mark/Space Decision Voltage Comparator W, applied to the circuit, steers the Mark or Space Command signal to the appropriate port.

The output of Transition Detector AE is also applied to Elapsed Time Monitor AC, which keeps track of the amount of time between transitions of the applied signal. If the time between transition exceeds a predetermined value, the Elapsed Time Monitor AC output actuates FET Switch Q2, placing the inputs to Mark and Space sample and hold circuits at ground, while the output from the Sample Command Decision circuit AA places the sample and hold circuits in a continuous sample state, thus forcing their outputs to also be at ground. The Buffer X prevents the ground applied via FET switch Q2 from affecting the signal fed to the inverting (negative) input of Mark/Space Decision Voltage Comparator W.

The threshold signal produced by the Reference Generator circuit AH is also applied to Reference Level Meter Drive circuit S. The circuit's dc output is routed to a reference level meter (selected function at the front panel - not shown) which indicates the amplitude and polarity of the threshold (reference) signal.

NOTE

The indication provided by the front panel meter (switched to indicate the threshold level) can be used as an aid in tuning the receiver to the incoming signal. Failure of the meter pointer to remain on a central reference point or to evenly oscillate about a reference point indicates the incoming signal is misaligned with the tone signals anticipated by the demodulator. The meter indication can also be used as an aid in adjusting the setting of Audio Balance Pot. R31.

4.4.2.6 Energy Detector, Radio Detector, and Carrier, Detect Voltage Comparator Circuitry Operation

The output pulses of the Transition Detector/Two Millisecond Delay Timer circuits (AE and AB) are fed to one input of Ratio Detector circuit AD, providing an indication of the time interval between successive transitions of the demodulated data. An enabling input to Ratio Detector AD is from the Energy Detector V which detects the energy level of the output signal from Differencing Amplifier Q, and provides an output signal indicative of whether the average energy of the input FSK audio signal is above or below a predetermined level. The output of the energy detector can be thought of as being in either of two binary states; Low State, when the energy level of the Differencing Amplifier Q output is above a fixed reference, and High State, when the energy level of the Differencing Amplifier Q output is below a fixed reference.

The output of Energy Detector V is applied to the Ratio Detector AD, in such a manner that when it is in low state, the Ratio Detector is enabled to examine the Transition Detector/Two Millisecond Delay Timer pulses applied to it over a continuous predetermined sampling period. The Ratio Detector then maintains a count which indicates the ratio of sampling periods in which the time interval between any two successive transitions fell within a predetermined minimum time interval to a total fixed number of sampling periods. This count is internally compared to a predetermined number to produce a binary output signal. When the count is less than this predetermined number, the output will be high, indicating a preliminary decision that a valid, information-carrying FSK input audio signal is being received. When the count is not less than the predetermined number, the output will be low, indicating a preliminary decision that a valid, information-carrying FSK input audio signal is not being received. When Energy Detector V output is in a high state, the output of Ratio Detector AD is low.

The output of Ratio Detector AD is passed through Lowpass Filter AF to the inverting (negative) terminal of Carrier Detect Voltage Comparator AG. The comparator compares the integrated Ratio Detector AD output with a predetermined reference signal voltage. Thus, the Ratio Detector AD and Threshold Voltage Comparator AG statistically process the demodulated data and provide an output signal when an incoming, information-carrying FSK audio signal has been detected. The comparator output signal is inverted (InverterU14-12-13) and its output (signal Detect High or SIGDETH) is utilized to actuated other receiver circuitry.

4.4.2.7 Demodulator Circuitry Detailed Theoretical Analysis

Subsequent paragraphs 4.4.2.8 through 4.4.2.18 comprise a detailed operational and theoretical analysis of the major demodulator circuits. Because of the large number of components and the complexity of Figure 7-3, Table 4-2 is included as an aid to define the circuits' location in Figure 7-3 and their component makeup.

Table 4-2. DEMODULATOR PWB A2 FUNCTIONAL CIRCUIT COMPONENT IDENTIFICATION

Circuit Name	Component Identification ⚠1
Ac-to-Dc Converter (Audio Meter)	C52; CR14, CR15, R140, R142, R146, R166; U45-5-6-7, U45-13-12-14
AGC Amplifier/Scaler	C51; CR13; R121 through R125, R127 through R136; U47-2-3-1, U47-6-5-7, U47-9-10-8
AGC Meter Drive	CR12; R169 through R171
Auto Start Relay Circuit Components	R159, R164, R165, U23-1 through -6; U39-10-11-13
Carrier Detect Voltage Comparator	C62; R157, R158, R160 through R163; U39-8-9-14
Data Control Components	U21-8-9-10, U24-3-4-5-6, U25-8-9-10, U26-8 through -13, U27-8-9-10
Differencing Amplifier	R67 through R70; U37-9-10-8
Elapsed Time Monitor	U22-1-2-8-10-11-12-16, U23-8 through -13
Energy Detector	C46; R98 through R101, R104, R105; U39-6-7-1
Input Buffer	R137, R138; U45-9-10-8
Input Lowpass Filter	C53 through C56, C58, C59, C63; R139, R141, R143 through R145, R147 through R151; U45-2-3-1, U46-2-3-1 U46-6-5-7
Mark Bandpass Filter	C37 through C41, C73 through C80; CR8; R30, R73 through R82, R172; U36-6-5-7, U36-10-9-8, U36-13-12-14 U44
Mark Detector	U21-8-9-10, U24-3-4-5-6, U25-8-9-10, U26-8 through -13, U27-8-9-10

⚠1 Reference designations are those of Figure 7-3.

Table 4-2. DEMODULATOR PWB A2 FUNCTIONAL CIRCUIT COMPONENT IDENTIFICATION (Cont.)

Circuit Name	Component Identification ⚠1
Mark Local Oscillator	Part of U1, U7, U8, U9, U10, U12; U11-12-9-10-11-13; U13-8 through -13; U14-8-9; U16, U17, U18
Mark/Space Decision Voltage Comparator	C45; R94 through R97; U39-4-5-2
Mark Tone Mixer	C21 through C25; R12 through R29; U36-2-3-1, U48
Ratio Detector	U25-12-13-11; U27-1-2-3; U31-1 through -6; U32 U33
Reference Level Meter Drive	R102, R103; R108, R109; U38-13-12-14
Sample and Hold Circuit Components (Part of Threshold Generator)	C47 through C50; CR9 through CR11; Q1, Q2; R106, R107, R110 through R116, R119, R120; U37-12-13-14, U40, U41
Sample Command Decision Circuitry (Part of Threshold Generator)	U14-11-10; U21-2-1-3; U21-5-6-4; U23-8 through -13; U24-12-11-13-10; U28-9-8-10; U28-12-13-11
Space Bandpass Filter	C31 through C35, C65 through C72; CR1; R49; R51 through R60, R173; U35-6-5-7, U35-10-9-8, U35-13-12-14, U43
Space Detector	C36; CR2, CR3; R61 through R66, R71; U37-2-3-1, U37-6-5-7
Space Local Oscillator	Part of U1, U2, U3, U5, U6; U11-2-5-3-4-1; U13-1 through -6; U14-4-6; U15, U19, U20
Space Tone Mixer	C26 through C30; R32 through R48, R50; U34, U35-2-3-1
Summation Amplifier	R72, R89, R90, R117; U38-9-10-8; VR1, VR2
Summation Amplifier Lowpass Filter	C43, C44; R91, R92
Transition Detector	U25-6-5-4; U26-1 through -6; U27-4-6-5; U29-1 through -6
Two Millisecond Delay Timer	U14-3-4; U28-1-2-3; U29-8 through -13; U30; U31-8 through -13
Voltage-Controlled Amplifier/Attenuator (Mixer Input)	C60, C61; CR16; Q3; R31, R152 through R156, R167, R168; U46-10-9-8

⚠1 Reference designations are those of Figure 7-3.

4.4.2.8 Detailed Operation of Differencing Amplifier U37-9-10-8 and the AGC Amplifier/Scaler Circuitry

Refer to Figure 7-3 and Table 4-2. Component U37-9-10-8 is a differencing amplifier with opposite-polarity inputs. A negative-polarity Mark Envelope input is applied to inverting input U37-9. A positive-polarity Space Envelope is applied to non-inverting input 37-10. As the inputs are balanced, the Mark and Space envelopes are essentially mirror images of each other (but in the opposite direction). They're also mutually exclusive in time. When a Mark Tone is present (at input U37-9) the amplifier output (U37-8) goes positive. The same output occurs when a Space Tone is applied (to input U37-10). The amplifier output (U37-8) then, is a relatively constant positive level.

NOTE

If the inputs were square waves, the amplifier output would be a pure dc level. The inputs, however, are ex potentials, and some noise exists on them and they're not exactly the same.

The output of the differencing amplifier is routed to the Energy Detector (U39-6-7-1) and, through a filter (consisting of R121 and C51) to the non-inverting input of op amp U47-9-10-8 of the AGC Amplifier/Scaler section.

4.4.2.8.1 AGC Amplifier/Scaler Circuit

NOTE

The AGC Amplifier/Scaler circuitry used in this demodulator is somewhat different than standard types. It is subsequently described in detail.

The reference voltage for op amp U47-9-10-8 is developed by resistors R122 and R123 placed across the + 12 Vdc power source. Feedback is through Resistor R124 to the junction of Resistors R122/R123. The non-inverted output signal (same polarity as the input signal at U47-10) is applied to a two op amp scaling network consisting of U47-6-5-7 and U47-2-3-1, via diode CR13, and to the unit's diversity gain connection via connectors J2-22/J4-11. The op amp network scales the signal's level and range to operate FET Q3 in a prescribed manner, in order to control gain.

NOTE

In this circuit, it is desired to make the level of the fixed voltage at U47-8 occur as a function of signal input. The reason for this is that when a diversity modem combination is used, it is desired to use the modem with the higher gain to control the gain of both modems. This method is sometimes referred to as "equal gain diversity".

To accomplish this, the signal is diode - ANDed by CR13 so that the higher level is the one that's seen by both modems.

The purpose, then, of the two op amp network is to match the AGC control voltage level at CR13 to the characteristics of the Voltage Controlled Amplifier.

4.4.2.9 Detailed Operation of the Transition Detector

When data makes a transition, that transition is applied simultaneously to the D input of flip-flop U26 (U26-5) and one input of Exclusive OR Gate U25 (U25-6). Prior to that time, the D and Q inputs of U26 (U26-5 and -1) were at the same state. This effected a low at gate output U25-4. As soon as data makes a transition to another state (regardless of what the original state was) gate output U25-4 goes high. The high is applied to the D input of Flip-flop U29 (U29-5). Some time later (within 7.8 milliseconds), the 128 kHz (applied at C input U29-3) makes a positive transition and triggers the Q output (U29-1) to a high state and Q output (U29-2) to a low state. This low is applied to one input of NOR Gate U27 (U27-6). As the other input to the gate (128 kHz) is high at the time, no transition appears at output U27-4. On the next half cycle of the 128 kHz pulse, gate output U27-4 goes high (both its inputs are low) and triggers Flip-flop U26 (U26-3). That action makes the D and Q inputs of U26 the same state. Consequently, the output of gate U25 (U25-4) goes low. When this occurs, the next positive transition of the 128 kHz clocks U29-2 (Q) low, thereby returning U27-4 to its low state. When the 128 kHz went high at that point, U27-4 went low. Just behind it, the other input (U27-6) goes high and keeps U27-4 low. Every time there is a data transition, we have one pulse out of U29-4 that is 7.84 sec wide. It does not matter in which direction the data is, as a pulse will be generated for all data transitions.

4.4.2.10 Detailed Operation of the Two Millisecond Delay Timer

When a data transition occurs, a pulse from the Q output of Flip-flop U29 (U29-1) is applied to one input of NAND Gate U28-2). No output (that is, change in output status) at the gate output (U28-3) occurs at the time, as its other input is low (due to the Q output of U29 [U29-13] being low). But, when the transition occurred, U29-11 is triggered by the trailing edge (low-to-high transition) of the pulse from Q output U29-2. In the meantime, the transition reflected in Q output U29-12 is applied to the reset input of Counter U30 (U30-11). That action removes the reset from U30 and it starts to clock. Approximately 2 milliseconds later, the Q9 output (U30-12) goes high and is applied to the D input of Flip-flop U31 (U31-9). One-half transition later of the 128 kHz, Q output (U31-13) changes to the high state, resetting Flip-flop U29 at U29-10. Q output U29-13 returns to low and Q output U29-12 goes high, resetting Counter U30. (U30 stops clocking and goes to zero).

If no data transitions occurred within the 2 millisecond period, no output at U28-3 will occur. But should a transition occur during this period, an output pulse will be present at U28-3.

4.4.2.11 Detailed Operation of the Ratio Detector

The ratio detector maintains a count that is a ratio of the number of 128 millisecond (7.8125 kHz) periods in which one or more data transitions occurred within 2 milliseconds of each other, to the total number of 128 millisecond periods considered. The number of 128 millisecond periods considered is eight. The ratio detector maintains a count that tells that out of the last eight 128 millisecond periods, how many of those periods contained transitions that occurred within 2 milliseconds of each other.

Observe Energy Detector U39 and its associated components. When insufficient energy is applied to the circuit, the output (U39-1) is high. The high zeros Shift Register U32, presets counter U33, and is applied as one input to NOR Gate U27 (U27-2), forcing its output (U27-3) low. This low signifies that no signal is present.

The initial count entered into the Counter U33 (prescaled input) is a binary 6 (that is 0110). (This number is the pattern of the counter's Q outputs. See Table 4-3. The counter remains in this preset condition until sufficient energy is applied to Energy Detector U39 to cause its output to change states. When this occurs, the reset of Shift Register U32 and the preset of Counter U33 are removed, and the circuit begins to function. When the energy detector output (U39-2) goes low, it could be assumed that a signal is present. The Q4 output of Counter U33 (U33-2) is low because of the preset condition.

Table 4-3. Operation of Shift Register A2 U32/Counter A2U33

State No.	Q Outputs Q4	Q3	Q2	Q1	
15	1	1	1	1	Excluded States
14	1	1	1	o	
13	1	1	0	1	
12	1	1	0	0	
11	1	0	1	1	No Signal
10	1	0	1	0	
9	1	0	0	1	
8	1	0	0	0	
7	0	1	1	1	Signal
6	0	1	1	0	Initial State
5	0	1	0	1	
4	0	1	0	0	
3	0	0	1	1	Excluded States
2	0	0	1	0	
1	0	0	0	1	
0	0	0	0	0	

Count Range

General Operation Description

(Refer to Paragraph 4.4.2.11 for detailed description)

A. If one or more narrow (2 millisecond) data pulses occur in any 128 millisecond (7.8125 Hz) period, a 1 (or high) is entered into Shift Register D input U32-7.

B. If the bit that emerges from Shift Register Q4 output (U32-2) is the same as that which entered, no change in Counter U33 Q4 input (U33-2) occurs.

C. If the bit that emerges from Shift Register Q4 output (U32-2) is different than that which entered, the count at Counter 33 will either be increased or decreased by one count.

D. As shown above, all states above 7 and below 6 indicate no signal and/or excluded states. States 6 and 7 imply signal presence.

With no pulses applied to Reset Input U31-4, the Q output (U31-1) will be high, but the Q output (U31-2) is routed to the shift register D input (U32-7). The shift register Q4 output (U32-2) will effect a high output at gate output U25-11/counter input U33-5, keeping the counter from counting (The counter will remain state 6 as previously described).

When a short time period between data transitions (less than 2 milliseconds) occurs, a pulse is generated and applied to the Reset Input of U31 (U31-4), resetting the flip-flop. (On the next transition of the 7.8125 Hz input, the flip-flop will be brought back to its original state.) When the transition of the 7.8125 Hz input went positive, it clocked a high into the shift register D input (U32-7). The Q output of U31 (U31-1), a low, is applied to one input of Exclusive OR U25 (U25-13). A low (0) from the Q4 output of the shift register (U32-2) is applied to the other gate input (U25-12). The low-low (0-0) input at the gate causes a low at its output (U25-11). This causes counter U33 to count.

The low at Counter Enable input U33-5 does not tell the counter in which direction to count, just to start counting. The information applied to Up/Down Input accomplishes this function. In this instance, the information applied at U33-10 is high, causing the counter to count upwards. That is, the first pulse applied at the Reset Input of U31 (U31-4), processed through the logic, causes the counter to count upwards (or, go from State 6 to State 7 - see Table 4-3).

NOTE

The timing involved is as follows: The clock that sets Flip-flop U31 back to its original state is the same clock that shifted the output of U31 into the shift register, and is not the same clock, in time, that causes Counter U33 to count up. That clock occurs one period later.

Refer to Table 4-3. If, in the intervening time, another pulse is applied to Up/Down input U33-10, the counter will count up to State 8. When this state occurs, Q4 input U33-2 changes state (goes high -changes to a "1"). This high, applied to gate input U27-1, forces a low output at U27-3. This indicates that the point has been reached that implies that no valid data exists. If another pulse were applied to Up/Down input U33-10, the counter would go to State 9, etc.

If a 128 millisecond-interval occurs in which there are no close data transitions, the counter will not count back to State 8. When this occurs, a "0" is applied to Shift Register U32 (at U32-7) and also a "0" is routed out of the device at the same time. This condition ("0" in and "0" out) means that the number of "1's" in the register has not changed - they shifted down by one place. Correspondingly, exclusive OR U25 inhibits counter U33 from counting (its output is high).

To recap the general operation of the shift register; the input to the register is a "1" if any two data transitions through the last time period were separated by less than two milliseconds. If no such data transitions were detected, the input to the shift register is "0". When the input and output of the shift register are the same, counter U33 is not run. When they're different, the counter is run. The difference is being constantly detected by Exclusive OR Gate U25.

When the operation progresses to the point where good data still exists (a "0" is still applied to the shift register input) but the register via internal shifting, outputs a "1", Exclusive OR Gate U25 will direct counter U33 to count. As before, the direction the counter will count (input U33-10) is determined by the input to the shift register (U32-7). When a "0" is applied to Up/Down input U33-10, the counter will count downwards.

To sum up the general basis for the shift register's operation; if a "1" is put into the Shift Register (U32-7), and a "0" is routed out of it, Counter U33 will count upward. If a "0" is put into the Shift Register and a "1" is routed out of it, Counter U33 will count downward. If the same bit comes out of the Shift Register as is put into it, be it either a "1" or a "0", Counter U33 will not count at all.

A "1" applied to the Shift Register (U32-7) is the result of at least 1 or more data transitions occuring within a 2 millisecond period over the entire 128 millisecond sample period. A "0" applied to the Shift Register indicates that there were no data transitions detected during that time.

4.4.2.12 Detailed Operation of the Threshold Lowpass Filter and Threshold Voltage Comparator

As previously stated, a low at the output of NOR Gate U27 (U27-3) would imply that no valid data exists. Conversely, a high would imply that valid data did exist. To clarify (decide) the validity of information present at gate output U27-3, the signal is analog-integrated (by Threshold Lowpass Filter R157 and C62) to average certain characteristics, and then applied to Threshold Voltage Comparator U39 (that is, U39-8-9-14 and its associated components. The output of the comparator (U39-14) is the resulting decision of this process. A low at this output implies valid data.

Note that the output of U39-14 is applied to the input of Inverter U14-13-12. In the remaining circuits of the unit, valid or detected data is referred to as a high. (As an example, the output of the inverter (U14-12) is routed out of the demodulator (at J1-12/J3-3) as SIGDETH (Signal Detect High) to the Interface Pwb A4.

4.4.2.13 Data Line Routing - Output of Mark/Space Decision Voltage Comparator U39-4-5-2

When a Mark State (low from Comparator U39-2) is applied to Inverter U14, the resulting high (U14-2) is applied to one input (U25-8) of Exclusive OR Gate U25. At the same time, the other input of the gate (U25-9) is low (unit is operating in Normal Mode). The gate output (high at U25-10) is applied to one input (U27-9) of NOR Gate U27. The resulting gate output (U27-10) is low, and is routed out of the demodulator (CRDTAL - CMOS Received Data Low at J1-18/J3-9).

If the front panel RECEIVE-SENSE-NORM/MARK HOLD/REV Switch A653 were placed in REV position, gate input U25-9 (the Normal line) will be high. As the other gate input (U25-8) is still high, a low results at the gate output (U25-10). Thus, the sense of the data is reversed, but all other transitions on the line remain the same. However, as gate output U25-10/succeeding NOR Gate input U27-9 is now low, the other gate input (U27-8) must be low, in order for the input at U27-9 to control the output at U27-10.

When NOR Gate input U27-9 is high, the high which is also applied to the Set (S) input of Mark Hold flip-flop U26 forces its Q output (U26-12) to remain low.

4.4.2.14 Detailed Operation of the Timed Mark Hold Circuit

If a condition existed where the units were in a Space State for an extended period of time, the teletype connected to the unit would continue to operate. A Mark Hold State, however, would keep the TTY from running under this circumstance. As previously described, if gate input U25-9 were high, and input U27-8 were low, the gate output (U27-10) would be a Mark Low. If the inputs to U27 were both low, the gate output would be a Space high. To accomplish the Mark Hold function, the Space State is allowed to continue (at U27-10) for a certain period of time.

To understand the timing of the Mark Hold circuitry, the following must be noted. The Q6, Q7, and Q8 outputs of Counter U30 (part of the 2 millisecond timer discussed in Paragraph the outputs referenced are U30-2-4 and -3, respectively) are applied as inputs to NAND Gate U24 (that is, U24-12, -13, and -11), producing a pulse at the gate's output (U24-10). Every time a data transition occurs, a pulse will emerge at gate output U24-10 providing the transition followed the previous transition by more than 2 milliseconds. That pulse, routed to Counter U22 via NOR Gate U27-13-12-11, will reset the counter (U22-11) to zero.

As previously stated, when a Space State exists, gate output U25-10/gate input U27-9 is low. This state would exist indefinitely, if no pulses were coming out of NAND Gate U24-10 (no pulses would indicate no data transitions had occurred). Also, no pulses would be applied to Counter U22 Reset Input (U22-11). At some point in time later, the Q9 output of Counter U22 (U22-12) goes high and clocks Flip-flop U26 (at U26-11), causing its Q output (U26-12) to go high. This high, applied to NOR Gate input U27-8 causes its output U27-10 to go low, and a Mark Hold condition results. To recap, a Mark Hold condition was imposed after a certain length of time after the last data transition. That period of time was fixed by Counter U22 and the clock rate applied to it.

4.4.2.15 Untimed Mark Hold Circuits Description

In the Timed Mark Hold circuit description, it was assumed that NOR Gate input U27-12 was high and input U27-13 was low in order to obtain a reset pulse for Counter U22 (at U22-11). These conditions are true during Normal operational mode.

If the front panel RECEIVE-SENSE-NORM/MARK HOLD/REV Switch A6S3 was placed in MARK HOLD position (that is, neither NORM nor REV position), the Normal Line connected to Exclusive OR Gate input U25-9 and NAND Gate input U21-9 would be high. The Reverse Line connected to NAND Gate input U21-8 would also be high. The highs applied to the inputs of gate U21 force a low output of U21-10. This low, applied to NAND Gate inputs U24-4 and -5, forces gate output U24-6 high, resetting Flip-flop U26 (at U26-10), establish a Mark Hold condition.

Another occurrence that effects a Mark Hold condition is associated with the output of Threshold Voltage Comparator U39-8-9-14. When invalid data is thought to exist, the comparator output (U39-14) is high, Inverter U14-13-12 output is low, and this low forces a high at the output of NAND Gate U24-3-4-5-6. The high, applied to the R input of Flip-flop U26 (U26-10) resets the flip-flop putting the unit in Mark Hold. Notice that if the S input of flip-flop U26 (U26-8) is also high, a Mark Data State results independent of the state of flip-flop U26.

4.4.2.16 Auto Start Relay Circuit Descriptive

In the description of the Timed Mark Hold Circuit, it was indicated that NOR Gate input U27-12 was high and input U27-13 was low in order to allow a reset pulse (via U27-11) to reset Counter U22. The reset pulse occurred when data transitions existed. This pulse also resets Flip-flop U23 (U23-4), causing its Q output (U23-2) to go high. The high is applied to the input of Current Amplifier U39 (at U39-10), causing its output to go low, closing the Auto Start Relay (K1, Figure 7-1). (The output of Current Amplifier U39 (ASDL - Auto Start Data Low) is routed to the relay via J2-10/J4-5).

In order to reopen the relay, where no data transitions exist, the Q12 output of Counter U22 (U22-1) will send out a positive transition to the C input (U23-3), causing it to change state. The clock pulse will occur approximately 30 seconds after the last data transition.

NOTE

Flip-flop U23, of course, can only be clocked if its R input (U23-4) is low. When no data transitions exist, it will be low.

When the Q output (U23-2) of Flip-flop U23 goes low, the resulting high at the current amplifier output (U39-13) will open the auto start relay.

4.4.2.17 Signal Processing and Operation of the Threshold Generator, including the Sample and Hold Circuits

NAND Gate output U24-10 is normally high, but contains a pulse (one pulse per data transition) that goes to a low state. (The trailing edge of this pulse occurs at 2 milliseconds, and the Pulse is 250 microseconds wide.) The pulse, inverted by Inverter U14-11-10, is simultaneously applied to one input of NAND Gate U21-5-6-4 (at U21-6) and one input of NAND Gate U21-2-1-3 (at U21-2). The remaining NAND Gate inputs, U21-5 and U21-1, correspond to the state of the data, and originate at the output of the Mark/Space Decision Voltage Comparator (U39-2) and Inverter U14-1-2 (U14-1), respectively. The output pulse will appear (inverted) at the output of whichever NAND Gate had a high input at that time. (Never simultaneously at both gate outputs). The gates, therefore, supply a pulse that is delayed by 2 milliseconds and steered by whatever the state of the input data line happens to be.

Every time a data transition occurs, Timing Flip-flop U23 (that is, U23-8-9-10-11-12-13) is reset (R input U23-10) by the same 250 microsecond pulse that is applied to NAND Gate inputs U21-6 and U21-2. Also, Counter U22 is reset to zero (via U22-11) at the same time. If no further data transitions occur, resulting in reset pulses, the counter continues its count forward from the last pulse. Approximately 0.5 second after the last data transition, the Q6 output makes a positive transition. This transition is applied to the clock input of Timing Flip-flop U23 (U23-11), causing its Q output (U23-12) to go low. This low is simultaneously applied to one input of NAND Gate U28-9-8-10 (at U28-8) and one input of NAND Gate U28-12-13-11 (at U28-13), thus forcing high outputs at U28-10 and U28-11.

Output highs, applied through appropriate resistor networks to the Sample and Hold Circuit Logic Inputs (U40-8 and U41-8) keep the circuits in their sample state, that is, the circuits outputs follow the signals applied to their analog inputs (U40-3 and U41-3).

When the $\overline{Q}$ output of Timing Flip-flop U23 (U23-12) went low, it also turned on transistor Q1 and FET Q2, pulling the inputs (U40-3 and U41-3) to ground (through Q2-S). Buffer U37-12-13-14 insures that action of pulling the sample and hold circuits inputs to ground will not interfere with the actual envelope being applied to the Mark/Space Decision Voltage Comparator U39-4-5-2.

When data transitions do occur often (compared to 0.5 second), Timing Flip-flop U23 remains reset because the Q6 output of U22 (U22-2) never arrives at a state where a positive transition, required to clock the flip-flop, occurs. Consequently, $\overline{Q}$ output U23-12 stays high, transistor Q1 and FET Q2 remain off, and the analog inputs to the sample and hold circuits (U40-3 and U41-3) are not affected. NAND Gate inputs U28-8 and U28-3 are both high, so the information present at NAND Gate outputs U21-4 and U21-3 is applied directly via appropriate resistor networks to sample and hold logic inputs U41-8 and U40-8, respectively.

NOTE

As previously stated, the information emerging from NAND Gate outputs U21-4 and U21-3 are mutually exclusive. This is also true, during normal operation, of the information emerging from NAND Gate outputs U28-10 and U28-11. The information, however, is inverted.

Circuit timing is such that the sample and hold circuit associated with Mark is told to sample while the signal envelope is high (corresponding to a Mark Tone) and the circuit associated with Space is told to sample while the signal envelope is low (corresponding to a Space Tone). In this manner, an average of both the high and low peaks of the signal envelope are presented at sample and hold outputs U40-5 and U41-5.

Capacitors C47, C48 and resistors R107 and R120 from a one-pole low pass filter. The filtered output is applied to the reference (positive) input of Mark/Space Decision Voltage Comparator U39-4-5-2 (at U39-5).

The filtered sample and hold output is also applied to the reference (positive) input of Meter Drive Buffer U38-12-13-14 (at U38-12). This buffer is used to drive a reference level meter that indicates how symmetrical, around a zero point, the output envelope is.

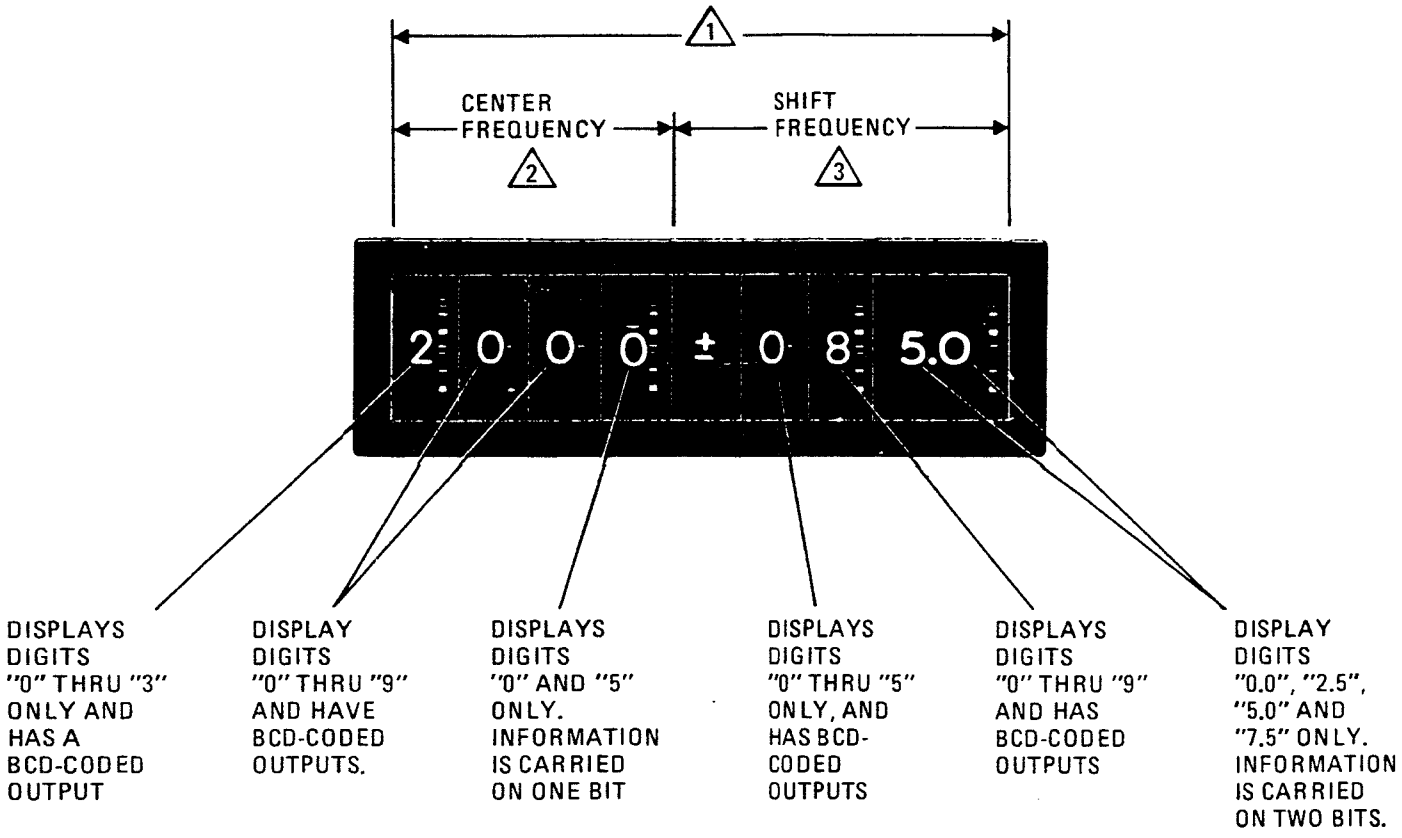
4.4.2.18 Mark and Space Local Oscillator Circuitry

Refer to Figure 7-3. The Mark Local Oscillator circuitry comprises Up/Down Counters U9 and U12, Hex D Flip-flops U7 and U10, Static Shift Registers U8 and U1, NOR Gate U11, Inverter U14, Type D Flip-flop U13, Phase-locked loop U16, Decoder Counters/Dividers U17 and U18, and their associated components. The Space Local Oscillator circuitry comprises functionally identical components. Operation of the counters, flip-flops, and shift registers is the same as that described for like components of the Timing and Control Pwb A3 (refer to paragraph 4.4.3). The output of the shift register is applied to the Comparator Input of Phase-Locked Loop U16 (at U16-3; U15-3 for Space Shift Register output). A 250 Hz input is applied to the Phase-locked loop signal input terminal (at U16-4 and U15-4). The applied frequency is multiplied by the loops so that their VCO outputs are 100 times the required frequency. The outputs are then divided by 100 by a two-divider network comprising U17 and U18 (Mark PLL output) and U19 and U20 (Space PLL output). The Mark Local Oscillator frequency output is applied to the Mark Tone Mixer at R12. The Space Tone Output is applied to the Space Tone Mixer R32. The tones applied are symmetrical square waves.

4.4.3 TIMING AND CONTROL PWB ASSEMBLY A3 AND FREQUENCY CONTROL BOARD ASSEMBLY A7 OPERATION DESCRIPTION

4.4.3.1 Frequency Processing - General Description

Figure 4-3 indicates the display digit, frequency limitation, and output coding characteristics of the front panel frequency selector switches (Frequency Control Board A7). Examine this illustration closely. Note that the Units of the Center Frequency (right-most center frequency selector switch) and limits of the Shift frequency are not independent of each other. The terminal provides a tone frequency between 270 Hz and 3400 Hz. If the center frequency were set at 3400 Hz, the shift would be set to zero. The same relationship applies to the lower end of the range. The important point is that the center frequency plus the shift should not exceed 3400 Hz, and that the center frequency minus the shift should not be less than 270 Hz.



NOTES:

1. MAXIMUM FREQUENCY (CENTER FREQUENCY + SHIFT) IS 3400 HZ. MINIMUM FREQUENCY (CENTER FREQUENCY - SHIFT) IS 270 HZ.

2. THE CENTER FREQUENCY IS LIMITED TO THE RANGE OF 270 HZ TO 3400 HZ. THE TOTAL NUMBER OF OUTPUT BITS IS ELEVEN.

3. THE SHIFT FREQUENCY IS LIMITED TO THE RANGE OF 0.0 TO 597.5 HZ (PLUS OR MINUS THE CENTER FREQUENCY). THE TOTAL NUMBER OF OUTPUT BITS IS NINE.

Figure 4-3. Frequency Selector Switch Technical Parameters

In addition to the other information given in Figure 4-3, note that the total number of output bits for the center frequency selector switches is 11 and for the shift frequency selector switches, 9 bits (total number of output bits: 20). The 20 output bits of the frequency selector switches are parallel-connected to Timing and Control Pwb A3. In the pwb, the numbers represented by the bits are converted to binary coded representation and subsequently divided by a factor of 2.5. A description of this conversion process follows:

a. The digits representing the tens, and higher digits of the input number preset a BCD Down-counter, while a Binary Up-counter is reset to zero.

NOTE

Tens digits in this scheme are interpreted as Units (are actually programmed in a units position), resulting in division by ten.

b. Both the BCD Down-counter and Binary Up-counter are clocked until the BCD Down-counter reaches zero.

c. The resulting bits, held in the Binary Up-counter, are subsequently parallel-loaded into the shift register two places to the left, that is; a bit weight of 2^m coming out of the counter will become 2^{m+2} at the shift register. At the same time, the two single bits representing 0.0, 2.5, 5.0, and 7.5 (the Units position of the Shift selector switch-supplied original number) are loaded in the 2^1 and 2^0 positions of the shift register. The resulting binary number is the original number divided by 2.5.

d. In the case of the center frequency, only one line represents 0.0 and 5.0 (the Units position of the Center Frequency selector-supplied original number - right most selector of that section). The same coding is used at the shift register as for the Units position of the Shift Frequency Selector, but the LSB (Least Significant Bit - 2^0) is always at ground. Consequently, the only binary number that can appear there is 0,0 or 1,0, representing (in that order) 0.0 or 4.0 Hz.

e. Example-Processing of a selected Center Frequency:

If the selected meter frequency is 1015 Hz:

- 101 is loaded into the BCD Down-counter
- The counters count to zero
- The binary number now reads: 001100101
- The resulting bits are parallel-loaded into the shift register. The resulting number is: 00110010110 = 406 = 1015/2.5

f. Example-Processing of a selected Shift Frequency:

If the selected shift frequency is 142.5 Hz:

- 14 is loaded into the BCD Down-counter
- The counters count to zero
- The binary number now reads: 001110
- The resulting bits are parallel-loaded into the shift register. The resulting number is: 00111001 = 57 = 142.5/2.5.

g. After parallel-loading the shift registers, the register contents are serially shifted through adders and subtractors, for arithmetic processing and subsequent routing to the phase-locked synthesizers.

The inputs from the frequency selector switches can be thought of as dc levels applied to the inputs of two sets of BCD Down-counters. (The center frequency BCD Down-counters are components U2 and U5. The shift frequency BCD Down-counter is component U10). The basic rate, or Epic Rate, that controls the whole timing sequence is the 0.977 Hz square wave output of Up-counter U16 (U16-4). That component, along with two section flip-flop U21, provides most of the timing references in the assembly.

4.4.3.2 Conversion Process Description

Refer to Figures 4-4 and 7-4. Note that component U16 is an up-counter (ripple counter). As it counts up (each stage of U16 is a binary ripple counter counting up) each stage makes a transition when the preceding stage makes a high-to-low transition. Consequently, every time the Q6 stage (U16-7, carrying the .977 Hz output) makes a transition (going high or going low), the lower order Q stages (carrying the higher frequencies) must be going low. This applies to the Q1 stage (U16-12) that carries the 31.25 Hz output.

Refer to Figure 4-5. When the.977 Hz square wave at the D input to U21 (U21-9) goes high (this point in time corresponds to the beginning of the Conversion Process), the C input of the same flip-flop section (U21-11) also goes high. (Actually, the C input goes high slightly before the D input - by the amount of time delay built into ripple counter U16). One time delay later, that is one period of 31.25 Hz, flip-flop U21's Q output (U21-13) follows the low-to-high transition of the .977 Hz input. Note that the 31.25 Hz waveshape shows a high-to-low transition at that time, which would seem to indicate that flip-flop U21 would not be triggered then. This, however, is not the case. Inverter U1-4-1-2 inverts the 31.25 Hz. The inverter output is then inverted again (by U17-1-2-3) and applied to the remaining clock input, U21-3. Consequently, Q output U21-1 goes high one-half cycle (of the 31.25 Hz input) later than Q output U21-13. The Q outputs are returned to their low state with the same relative timing following the high-to-low transition of the .977 Hz square wave. Each high-to-low transition of the .977 Hz square wave corresponds to the beginning of the Loading and Reset Period, where parallel-loading of the shift registers and adder resetting to zero takes place (as shown, this period occurs just prior to the Read Period).

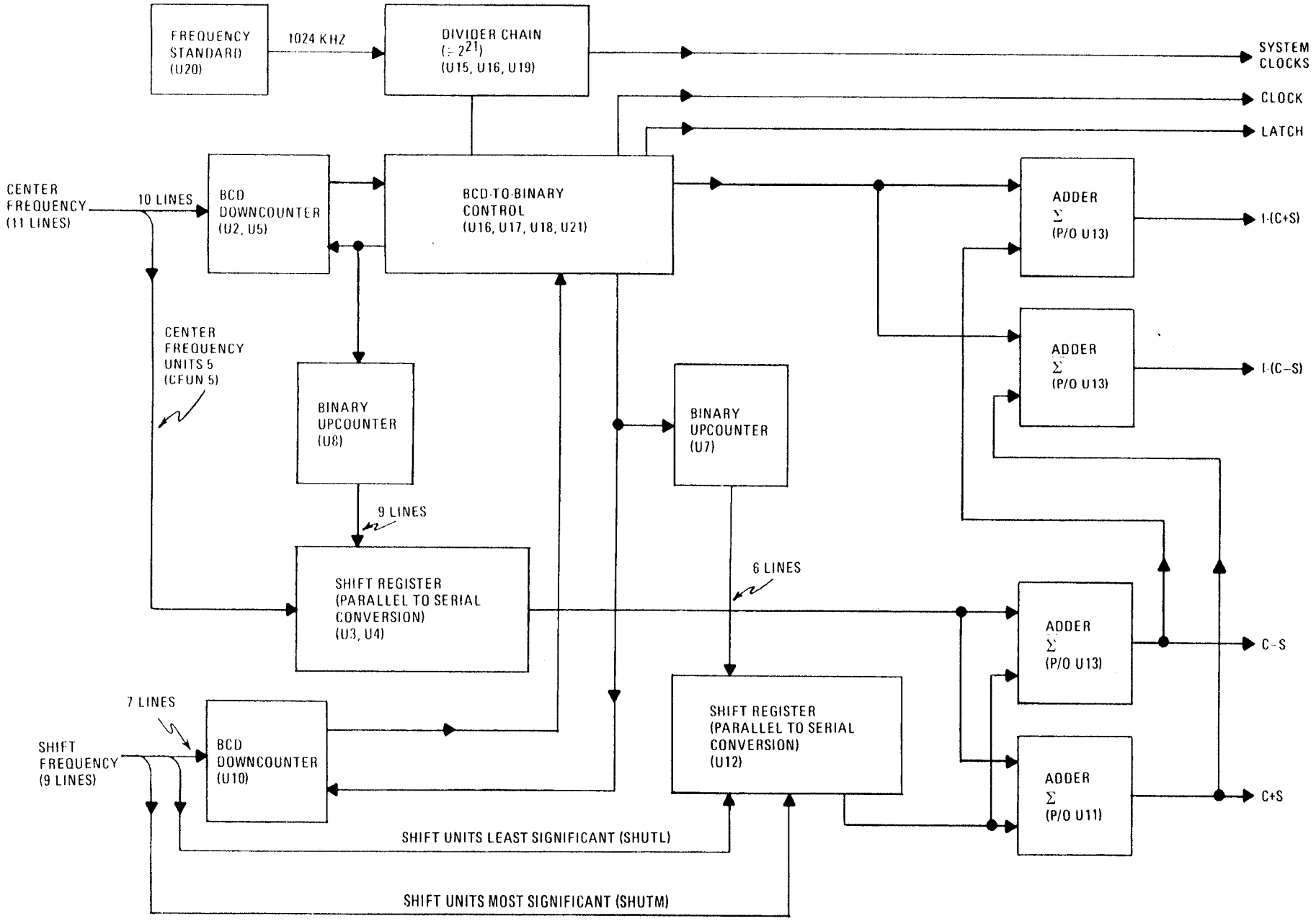


Figure 4-4 Timing and Control Pwb Assembly A3 Functional Block Diagram

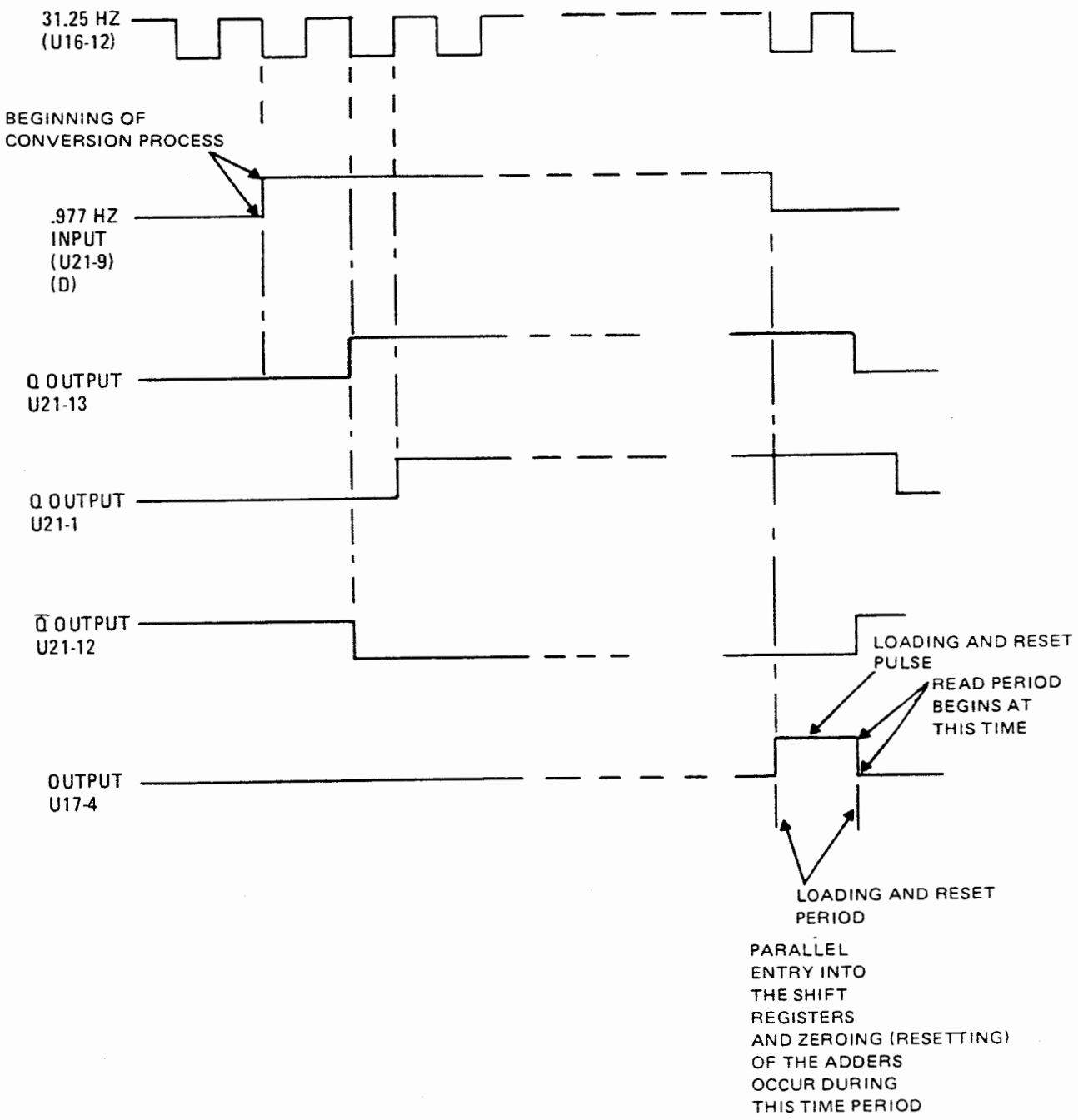


Figure 4-5. Conversion Process Waveform Data

Refer to Figure 4-5. When the.977 Hz square wave at the D input to U21 (U21-9) goes high (this point in time corresponds to the beginning of the Conversion Process), the C input of the same flip-flop section (U21-11) also goes high. (Actually, the C input goes high slightly before the D input - by the amount of time delay built into ripple counter U16). One time delay later, that is one period of 31.25 Hz, flip-flop U21's Q output (U21-13) follows the low-to-high transition of the .977 Hz input. Note that the 31.25 Hz waveshape shows a high-to-low transition at that time, which would seem to indicate that flip-flop U21 would not be triggered then. This, however, is not the case. Inverter U1-4-1-2 inverts the 31.25 Hz. The inverter output is then inverted again (by U17-1-2-3) and applied to the remaining clock input, U21-3. Consequently, Q output U21-1 goes high one-half cycle (of the 31.25 Hz input) later than Q output U21-13. The Q outputs are returned to their low state with the same relative timing following the high-to-low transition of the .977 Hz square wave. Each high-to-low transition of the .977 Hz square wave corresponds to the beginning of the Loading and Reset Period, where parallel-loading of the shift registers and adder resetting to zero takes place (as shown, this period occurs just prior to the Read Period).

4.4.3.3 Counter Initialization

From the previous paragraphs, and Figure 4-5, it was indicated that whenever the .977 Hz square wave went high (low-to-high transition), the Q outputs of flip-flop U21 followed one period of the 31.25 Hz input (U21-13) and then an additional half-period at U21-1 later. Also, the output of NOR Gate U17-5-6-4 (U17-4) was low at that time.

Pin 9 of the Center frequency BCD Down-counter U2 (and also shift frequency BCD Down-counter U10) is its asynchronous reset enable input, and is connected to Q output U21-1. A low at U2-9 (or U10-9) enables the preset inputs to establish the state of the counter. Remember that prior to the .977 Hz input going high (negative-to-positive transition), the input line at U2-9 (and U10-9) was low (reflecting the low at Q output U21-1). After the .977 Hz input goes high, the preset line also goes high, removing the preset condition. When this occurs, the counter is enabled (ready to be clocked).

Pin 1 of BCD Down-counter U5, the remaining portion of the center frequency BCD Down-counter, has the same significance as Pin 9 of U2, but operates at the opposite polarity. Its input, therefore, is from Q output U21-2. Therefore, at that point in time (1-1/2 periods of the 31.25 Hz input after the low-to-high transition of the .977 Hz square wave, the jamming inputs to the BCD Down-counters (U2, U5 and U10) have been removed.

The preset enable signal applied to Pin 1 of BCD Down-counter U5 is also applied to Binary Up-counters U8 (U8-11) and U7 (U7-2), which resets both Binary counters to zero at the time the BCD counters are preset to their initial count.

NOTE

Any change of the frequency selector switches at that point in time would not register in the counters.

4.4.3.4 Counter Clocking

When Q output U21-1 went high, the high was also applied to one input of NAND Gate U6 (U6-13; also U6-2). That high allows the gate to be operated or controlled by its other two inputs (U6-11 and 12 or U6-1 and 8).

Input U6-12 (and U6-1) represents the final output of the BCD Down-counter. That output (input to U6) is high whenever the count is greater than zero. If it is assumed that the number in the counter is not zero, then the U6-12 (and U6-1) input is high.

With both inputs U6-12 and U6-13 (or U6-1 and U6-2) high, the 1000 Hz input constantly present at input U6-11 (or U6-8) acts as the clock (through U6-10 and U6-9) for the BCD Down-counters (at U2-1, U5-15 and U10-1), and the Binary Up-counters (at U8-10 and U7-1).

The 1000 Hz input clocks the BCD Down-counters down, and Binary Up-counters up until the BCD counters count reaches zero. When that happens, their output lines (Carry-Out Lines U2-14 and U10-14) go to zero and stop the clock from running (via the U6 NAND gate action previously described). The binary equivalent of the BCD numbers previously loaded into the BCD counters is now available at the Binary Counter's output, and will remain so.

4.4.3.5 Conversion Time Description

Conversion time is a function of the size of the number entered in the BCD Down-counters (the smaller the number, the quicker the conversion etc.). Numbers are always converted between the low-to-high and high-to-low transitions of the .977 Hz input. As previously described, when the conversion is complete, the clock will be shut off and the binary counters will retain the numbers entered until the next low-to-high transition of the .977 Hz input. When the intervening high-to-low transition occurs, the number is parallel-loaded into the shift registers during the Loading and Reset Period - see Figure 4-5. At the end of the Loading and Reset Period, the Read Period will commence.

4.4.3.6 Loading and Reset Period

Refer to Figure 4-5. During the Conversion Process, the output at NOR Gate U17-4 is low. This is due to the presence of a low at one of its inputs, U17-5, and a high on the other, U17-6.

After the end of the Conversion Process, at the next positive-to-negative transition of the .977 Hz pulse, the output at NOR Gate U17-4 goes high for a time equal to one cycle or period of the 31.25 Hz input. This high, applied at the inputs of the shift registers (specifically, at U3-9, U4-9 and U12-9) parallel-loads them with the numbers held in the binary counters. This entry or loading can occur only at this time (referenced as the Loading and Reset Period on Figure 4-5).

NOTE

The shift registers operate in serial mode except during the parallel-loading period just described.

The low, present at U17-4 during parallel-loading of the shift registers, also resets or zeros adders U11 and U13 during that time.

4.4.3.7 Read Period Timing

The Read Period starts at the trailing edge of the pulse generated (by U17-4) to accomplish shift register parallel loading and reset functions (refer to the Loading and Reset Period in Figure 4-5). From the previous discussion, remember that when the .977 Hz input makes a transition, Q output U21-13 follows the transition one period of the 31.25 Hz input later; Q output U21-1 follows the tran-

sition one-half period of the 31.25 Hz input later (that is, Q output U21-1 follows any transition of the .977 Hz input 1-1/2 periods of the 31.25 Hz input later, as shown in Figure 4-5). In brief, all that the outputs of both sections of flip-flop U21 do is produce delayed versions of the .977 Hz input.

The output at NOR Gate U17-4 is high only during the Loading and Reset Period, as previously described and shown in Figure 4-5. As previously stated, parallel-loading of the Shift Registers (U3-U4 and U12) and zeroing of adders (U11 and U13) take place during this time.

The clock pulses that shift all the data out of the shift registers, through the adders, and finally out the ports of the circuit (serial mode clocking) are supplied by the output of NOR Gate U17-12-13-11. Note that the two inputs are 31.25 Hz (at U17-12) and the one and one-half period of the 31.25 Hz delayed version of the .977 Hz square wave (at U17-13).

When this input (U17-13) goes low, the other 31.25 Hz gate input (U17-12) will appear (inverted) at the output U17-11. That output appears to look like a clock of the 31.25 Hz input. The first transition of this clock occurs two 31.25 Hz periods after the positive-to-negative of the .977 Hz input. This clocking of the shift registers (applied at U3-10/U4-10 and U12-10) will continue until the Conversion Process is re-initiated. (At that time, input U17-13 will go high and the clocking will cease.) As stated, the Conversion Process will commence with the next negative-to-positive transition of the .977 Hz input.

4.4.3.8 Read Period Data Interpretation

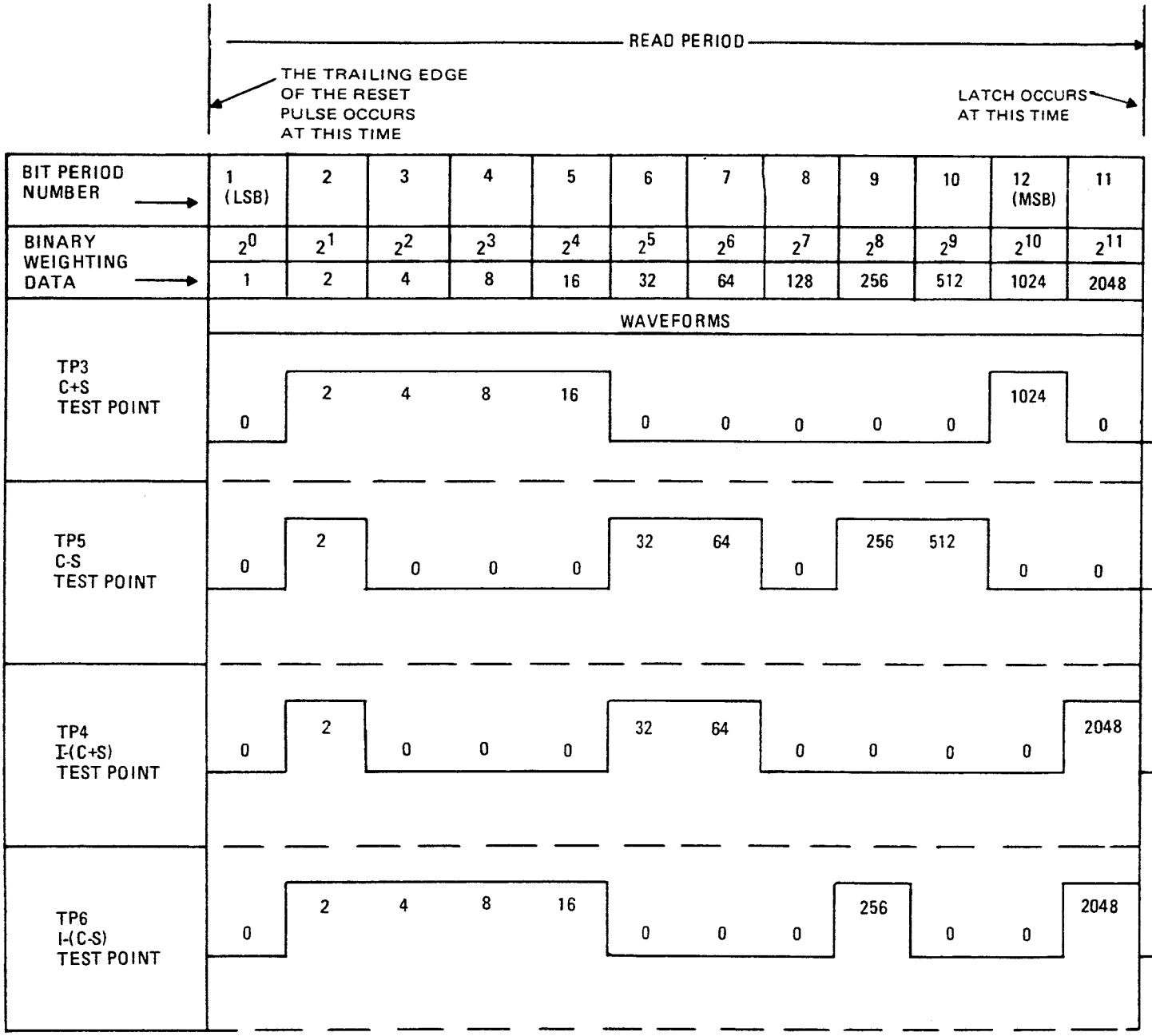
Figure 4-6 shows typical data output sampled during the Read Period. Note that only the first 12 bit periods of the Read Period are used. Latching is timed to occur at the end of the twelfth bit, and the rest of the Read Period is not used. The Shift Register clock will continue to run until the commencement of the next Conversion Process.

The bit period number, binary weighting, selected test point waveform data, and calculations are described in Figure 4-6. Study this information carefully to properly interpret circuit outputs.

4.4.3.9 Description of Latch Timing

The latch, as previously stated, is timed to occur at the end of the twelfth bit period of the Read Period. The purpose of the Latch is to indicate, to the receiving unit that only the previous twelve bit periods (the Read Period) are the valid data to be used. Data received either side of this Read Period is invalid.

The latch function is generated by dual flip-flop U18 in response to various input conditions supplied. Refer to Figure 4-7 and Figure 7-4. Note that the Data Sampling Points occur at the half-period points of the 31.25 Hz input (U18-3). When the 3.90 Hz input (U18-11) goes high at the end of the eleventh bit period, Q output U18-13/D input U18-5 will also go high. Latch output Q (U18-1) will go high one period of the 31.25 Hz clock later (which is one-half period in time after the last data sampling point). This low-to-high transition at Q output U18-1 effects the latch. Both Q outputs (U18-13 and U18-1) remain high until they are reset to the low condition by the .977 Hz output of U21-13.



CALCULATIONS:

- CENTER FREQUENCY (C) = 2400 HZ
- SHIFT FREQUENCY (S) = ±235.0 HZ
- I FREQUENCY (LOCAL OSC.) = 8000 HZ
- TP3 SHOULD DISPLAY C+S; C+S = 2400 + 235 = 2635 HZ
- TP5 SHOULD DISPLAY C-S; C-S = 2400 - 235 = 2165 HZ
- TP4 SHOULD DISPLAY I-(C+S); I-(C+S) = 5365 HZ
- TP6 SHOULD DISPLAY I-(C-S); I-(C-S) = 5835 HZ

A. FOR TP3; 2+4+8+16+1024 = 1056; 1056 x 2.5 = 2635 HZ = C+S
B. FOR TP5; 2+32+64+256+512 = 866; 866 x 2.5 = 2165 HZ = C-S
C. FOR TP4; 2+32+64+2048 = 2146; 2146 x 2.5 = 5365; 8000 - 5365 = 2635 HZ = I-(C+S)
D. FOR TP6; 2+4+8+16+256+2048 = 2334; 2334 x 2.5 = 5835; 8000 - 5835 = 2165 = I-(C-S)

Figure 4-6. Typical Data Output and its Interpretation During Read Period

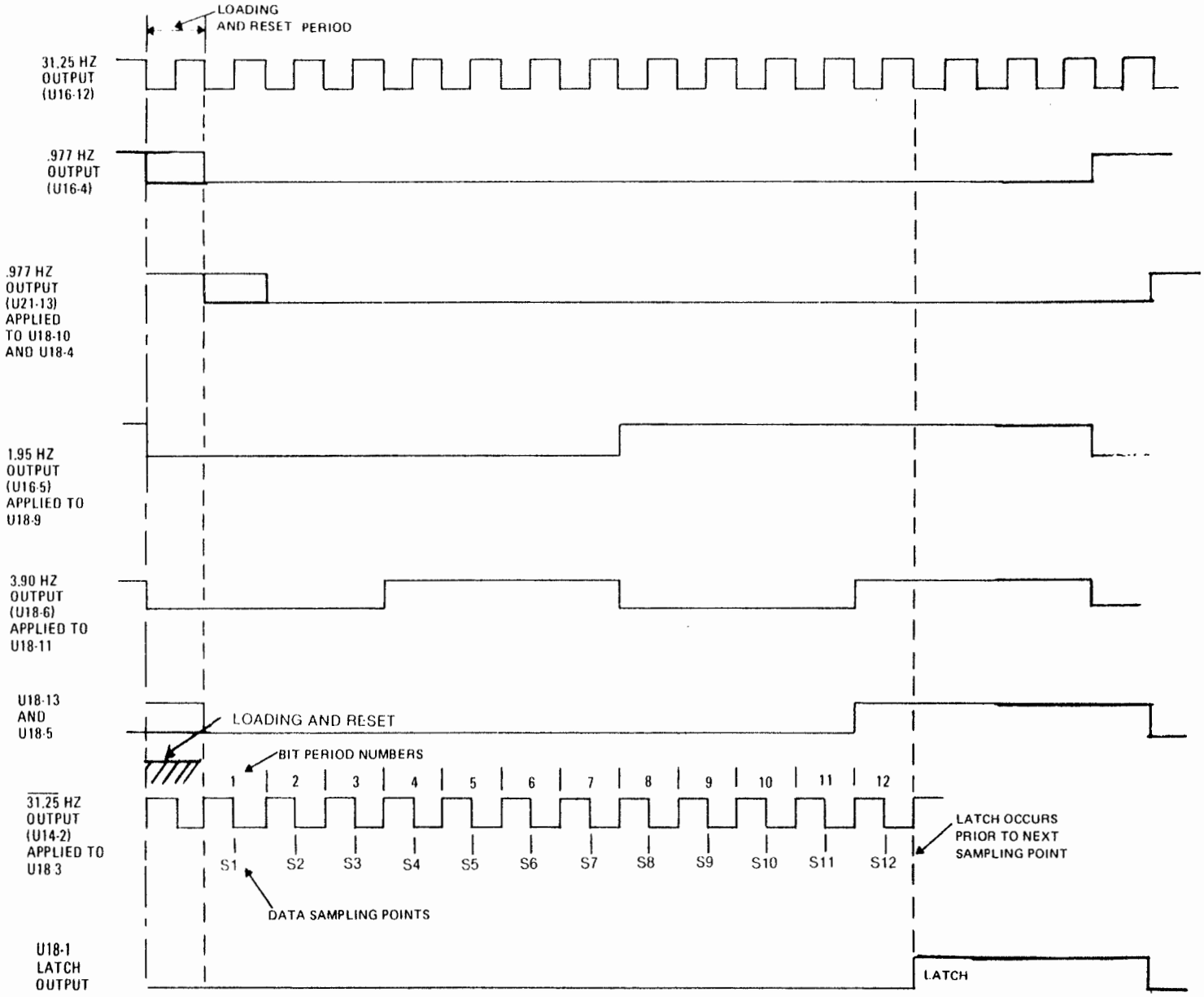


Figure 4-7. Latch Timing Relationships

4.4.3.10 Production of the I, C+S and C−S Outputs

Refer to Figure 4-8. Note the timing relationship and binary weighting of the waveforms present adder parts U11-14 and U11-15. As calculated in the illustration, these two inputs are added to produce an output waveform at port U11-1 representative of 8000 Hz. This is the I, or Local Oscillator, frequency referenced in Figure 4-6.

Refer to Figure 7-4. The center frequency and shift frequency input are applied at adder ports U11-10 and -13, and U11-11 and -12, respectively. These inputs are added in U11 to produce the C+S (Center Frequency plus Shift Frequency) at port U11-9. (This is the C+S waveform referenced at TP3 in Figure 4-6.) An inverted version of this output, C+S is present at port U11-4.

Refer to adder U13 in Figure 7-4. The 8 kHz output of adder U11 (U11-1) is applied at ports U13-10 and -13. The inverted C+S output of adder U11 (U11-4) is applied at port U13-11. The center frequency and an inverted version of the shift frequency are applied to at ports U13-15 and U13-14, respectively. Processing in the adder produces an I – (C+S) output at port U13-9, a C−S (Center Frequency minus Shift Frequency) output at port U13-1. The C−S output at port U13-1 is inverted and applied to U13-12 to produce the I – (C−S) output at port U13-4. Interpretation of the output waveforms at these ports is given in Figure 4-C (TP3, TP4, TP5 and TP6 waveform data).

4.4.3.11 Production of Other Frequency Outputs

Refer to Figure 7-4. The frequency standard for all of the frequencies produced in the assembly is 1.024 MHz standard U20. The standard is followed by a three component, ripple counter-type divider chain, U19, U15 and U16.

U19 is a divide-by-128 ripple counter that produces output frequencies of 8 kHz, 16 kHz, 32 kHz, 64 kHz, and 128 kHz at ports U19-3, -4, -5, -6 and -9, respectively.

Besides producing the 1 kHz clocking frequency at U15-9, divider U15 produces 62.5 Hz, and 500 Hz outputs at U15-3, -5 and -6, respectively.

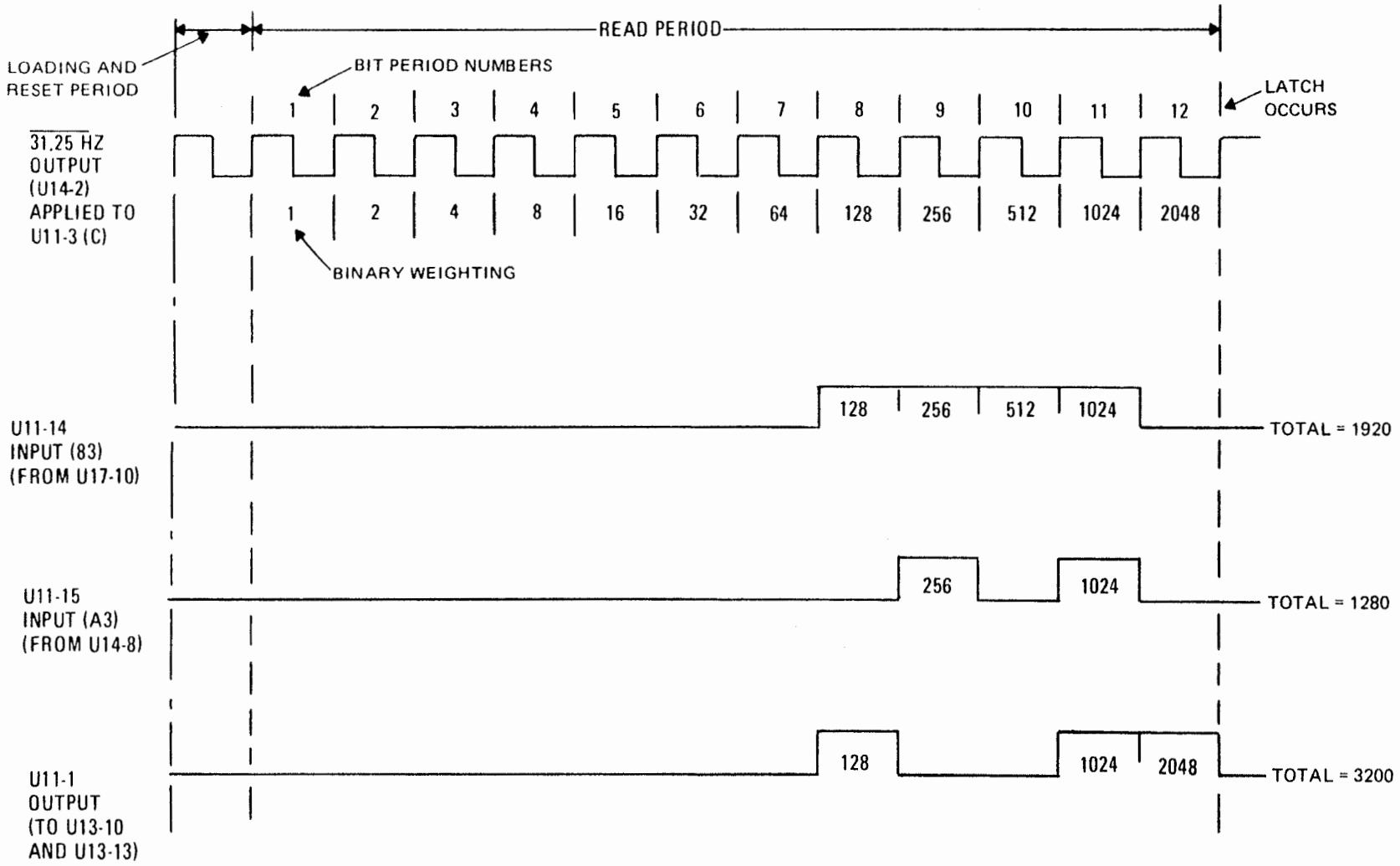
Divider U16 produces the .977 Hz, 31.25 Hz frequency outputs usage (previously described) at ports U16-4 and -12, respectively. The divider also produces 1.96 Hz, 3.9 Hz, and 7.81 Hz outputs at ports U16-5, -6 and -9, respectively.

4.4.4 INTERFACE PWB ASSEMBLY A4 OPERATION DESCRIPTION

4.4.4.1 Input Loop Circuitry Description

Figure 4-9 is a functional block diagram of Interface Pwb A4. Figure 4-10 is a simplified diagram of the input loop circuitry. From this illustration, note that the Regulator circuit is connected across diode bridge pins U1-1 and -2 that the load is in series with the bridge, connected to U1-4. The rectified current passing through the regulator is split between resistor A4R2 and the front panel meter 1M1. The meter's deflection is calibrated to read the total loop current by the INPUT LOOP METER CAL. potentiometer A4R1.

The Regulator is a two-transistor constant current type. It's current is fixed by INPUT LOOP ADJUST potentiometer A5R2 (refer to Figure 7-5).



CALCULATIONS:

1920 HZ x 2.5 = 4800 HZ (U11-14)
1280 HZ x 2.5 = +3200 HZ (U11-15)
8000 HZ

3200 HZ x 2.5 = 8000 HZ (U11-1)

8000 HZ REPRESENTS THE I OR LOCAL OSCILLATOR FREQUENCY

Figure 4-8. Production and Interpretation of the 8 kHz I (Local Ocillator) Frequency

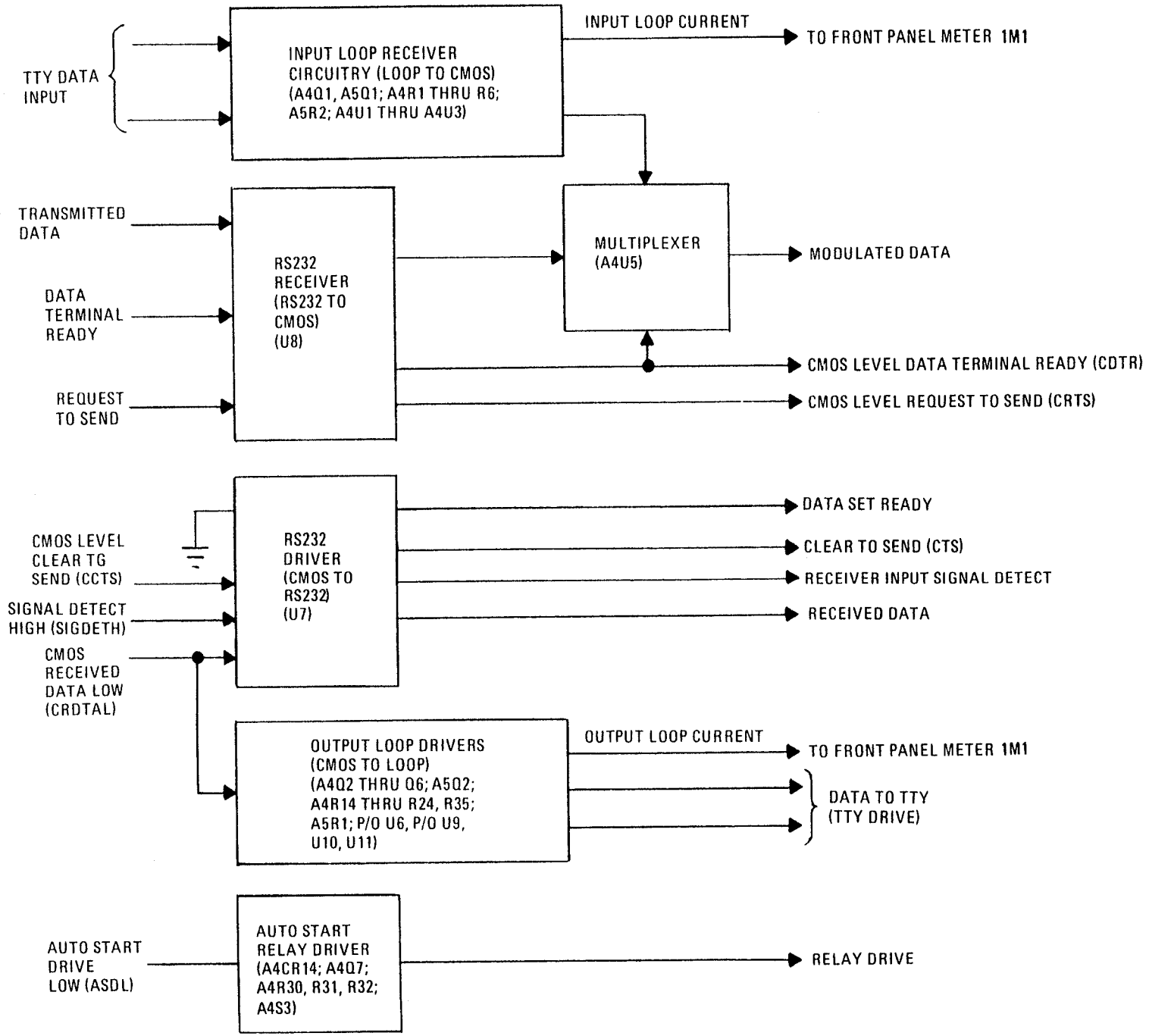


Figure 4-9. Interface Pwb Assembly A4 Functional Block Diagram

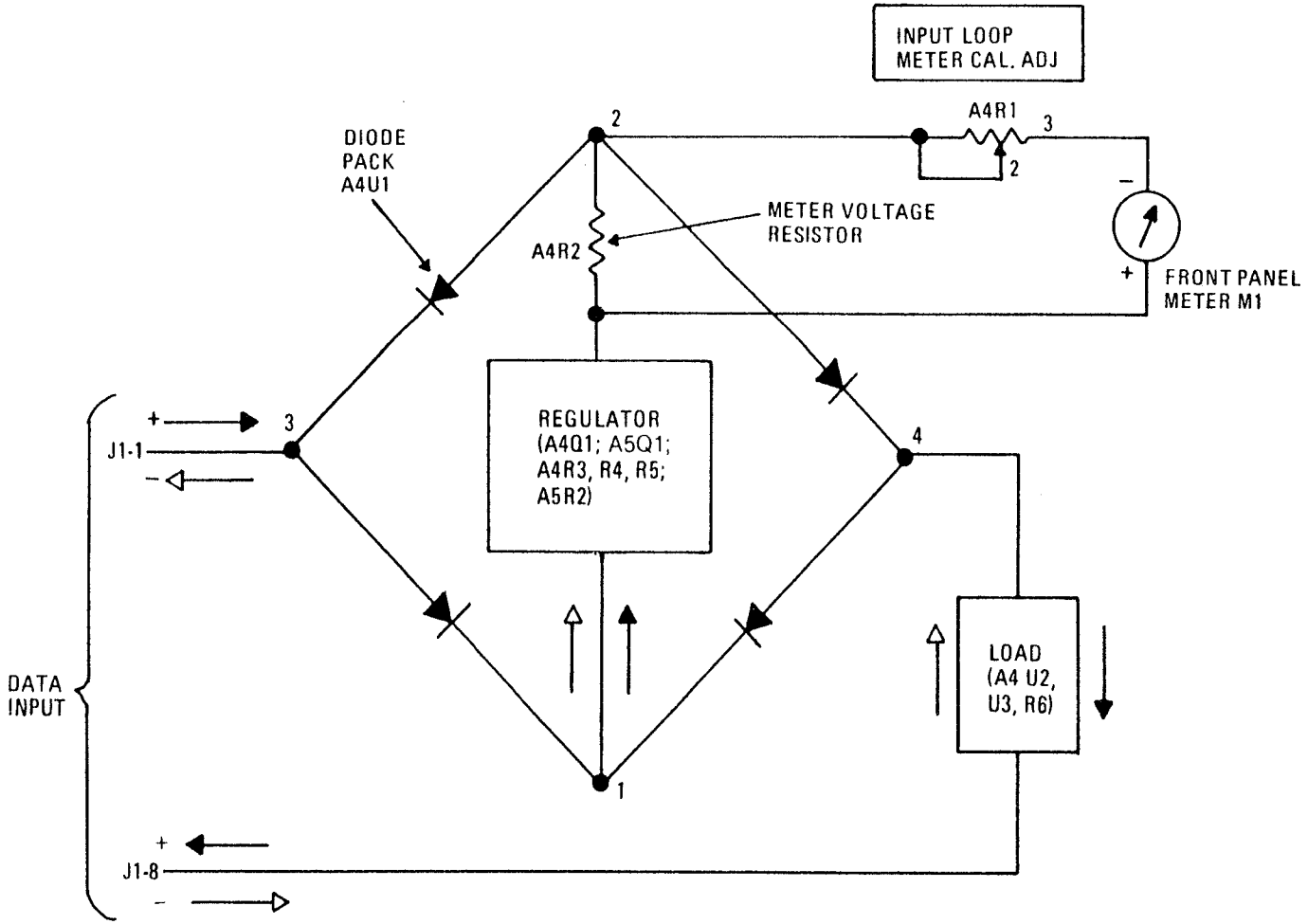


Figure 4-A. Interface PWB A4 Input Loop Circuitry

Figure 4-10. Interface PWB A4 Input Loop Circuitry

The Load, as shown in Figures 4-10 and 7-5, consists of optical isolators U2 and U3 shunted by resistor R6. From Figure 7-5, note that U2 and U3 are connected in reverse order. The diodes within their outlines will aid in understanding their operation.

Another control that is part of the input circuitry is NEUTRAL/POLAR switch S1. This switch controls Multiplexer U5, as subsequently described.

4.4.4.2 Receiver Circuit Operation - Neutral and Polar Modes

The receiver circuitry consists of optical isolators U2 and U3, NAND Gates U4-1-2-3, U4-5-6-4, U4-8-9-10, and Multiplexer U5. Gate outputs U4-3 and U4-4 are the receiver inputs to Multiplexer U5 (U5-6 and -5, respectively).

4.4.4.3 Operation in Neutral Mode

To review, Neutral Mode operation dictates that the current be entirely ON or entirely OFF. Referring to Figure 7-5, current might be applied into J1-1 and out J1-8, or vice versa. But the current does not cross over, that is, it does not change direction in Neutral Mode. The two possible states then are current-flowing and not-current-flowing.

If the equipment were connected such that J1-1 was more positive than J1-8 (current flowing in J1-1 and J1-8), the diode of U2 will be forward-biased while the diode of U3 will be reverse-biased, thereby allowing forward current to pass through U2 only.

When current passes through the diode of U2, it turns on an internal integral transistor that makes the resistance between U2-5 and U2-4 very small. Consequently, the voltage at U2-5 goes almost to ground, thereby applying a low logic level to NAND Gate input U4-6, resulting in a high output at U4-4. When the current stops, gate input U4-6 goes high, and gate output U4-4 goes low. Note that since U3 is essentially inactive, gate input U4-5 is always high during this operation.

If the equipment were connected such that J1-8 was more positive than J1-1 (current flowing in J1-8 and out J1-1), the diode of U3 will be forward-biased, while the diode of U2 will be reverse-biased, thereby allowing forward current to pass through U3 only.

When current passes through the diodes of U3, it turns on an internal integral transistor that makes the resistance between U3-5 and U3-4 very small. Consequently, the voltage at U3-5 goes almost to ground, thereby applying a low logic level to NAND Gate input U4-5, resulting in a high output at U4-4. When current stops, gate input U4-5 goes high, and gate output U4-4 goes low. Note that since U2 is essentially inactive, gate input U4-6 is always high during this operation.

From the previous discussion, it is apparent that Neutral Mode operates independent of the direction of current flow.

4.4.4.4 Operation in Polar Mode

To review, in Polar Mode operation, the direction of current changes. For reference, assume that positive current flow is that current that will flow when input J1-1 is more positive than J1-8; negative current flow will be just the opposite.

When input J1-1 is more positive, optical isolator output U2-5 goes low. Optical isolator output U3-5, however, is still high (refer to the discussion concerning these isolators in paragraph 4.4.4.3). The U2-5 low is applied to NAND Gate input U4-2, forcing its output, U4-3, high. As shown, output U4-3 is connected to input U4-9 and, as optical isolator output U3-5 is high at this time, gate output U4-10 is low. Output U4-10 is cross-coupled to input U4-1, reinforcing the state of that gate. If the current is removed, the state of the flip-flop (U4-1-2-3 and U4-8-9-10) does not change.

When the current reverses itself, optical isolator output U3-5 goes low and output U2-5 will go and remain high. The low at U3-5 is reflected at gate input U4-8, forcing output U4-10 and input U4-1 high. Input U4-2 is already high so the flip-flop changes state to the other direction and remains that way until current direction again changes.

4.4.4.5 Selection of Neutral or Polar Modes - Operation of Multiplexer U5.

Selection of either Neutral or Polar Mode operation is effected by NEUTRAL/POLAR Switch S1, which controls the inputs to Multiplexer U5. Multiplexer U5 has two control inputs (U5-14 and -2) and four other input lines.

To understand the operation of U5, both input control lines have to be considered. NEUTRAL/POLAR Switch S1 controls input U5-14. The other control input U5-2, allows the multiplexer to be controlled by either the RS-232 protocol data terminal ready or PSDTR (Pseudo Data terminal Ready) inputs. Note that only three of the four remaining multiplexer inputs are used; U5-6, U5-5 and U5-3/4 (tied together).

The data associated with RS-232 protocol is applied to input U5-3/-4. If control input U5-2 is high, information at that input will pass through the multiplexer to output port U5-7. To pass data associated with a current mode (as opposed to RS-232, which is a voltage mode), control input U5-2 has to be low. When NEUTRAL/POLAR switch S1 is in NEUTRAL position, multiplexer input U5-14 is high, and assuming U5-2 is low, allows data present at U5-5 to go through the multiplexer. When NEUTRAL/POLAR switch S1 is in POLAR position, multiplexer input U5-14 is low, and assuming U5-2 is low, data present at U5-6 will pass through the multiplexer.

4.4.4.6 Receive Protocol Description

Refer to Figure 7-5. Component U8 is an RS-232 Line Receiver whose inputs are compatible with RS-232 electrical specifications. The output signals of the receiver are compatible with the CMOS logic levels used in the assembly.

The Transmitted Data input is, as shown, applied to input U8-13. The inverted output, U8-11, is applied to multiplexer U5 at U5-3/4. At the same time, a high level Data Terminal Ready input is applied to U8-1, providing a CMOS low output at U8-2.

NOTE

In RS-232 protocol, data originates at a Data Terminal. A high level Data Terminal Ready input is always high; indicates that the terminal is on-line and ready to send information.

The low output U8-3 is applied to NAND Gate input U4-12, making output U4-11 and multiplexer input U5-2 high. Multiplexer input U5-14 will have no effect, because when U5-2 is high, the state of U5-14 determines whether the input of U5-3 or U5-4 will pass through the multiplexer. As inputs U5-3 and -4 are tied together, the state of input U5-14 is not significant.

The Pseudo Data Terminal Ready (PSDTR) Mode has been included to allow data to be input at RS-232 levels without going through the entire RS-232 protocol. When PSDTR switch S2 is placed in PSDTR position, the resulting low is applied to U4-13, forcing a high at output U4-11/input U5-2. The effect on the multiplexer is the same as if the legitimate Data Terminal Ready signal were applied.

The Request-To-Send (RTS) signal, applied at gate input U8-4, is sent to the modem, and indicates the data terminal would like to send information. The data terminal will respond, after a certain length of time, with a Data Set Ready signal. (The Data Set Ready Signal indicates that the link is ready to transmit data.) The Request-To-Send signal is applied at U8-4. The output at U8-6 is inverted by inverter U9-9-8, and routed out of the assembly (via J1-18) to the modulator. Also, the Data Terminal Ready signal at U8-3 is inverted (by inverter U9-11-10) and also routed to the modulator (via J1-17). (This signal indicates [to the modem] that the terminal is to be used in the RS-232 mode.)

Note that placing the unit in Pseudo Data Terminal Ready mode does not affect the inverter output U9-10. Consequently, when PSDTR is used, the modulator will respond to data via U8-13 (RS-232 voltage levels) without requiring satisfaction of RS-232 protocol. The output of multiplexer U5 (U5-7) is routed out of the assembly at J1-16 (MOD. DATA).

4.4.4.7 Output Loop Driver Functional Analysis

Refer to Figures 4-11 and 7-5. The two output loop drivers, Driver A and Driver B, can be thought of as functioning like two mutually-exclusive switches.

When the Signal applied to the drivers (from J1-13) is high, corresponding to space data present, Driver A is the active driver. The signal is inverted by buffer/inverter U6-11-12 and the resulting low is applied to optical isolator U10 (at U10-2). An internal diode, connected across U10-1-2, conducts turning on (or saturating) an internal transistor connected across U10-4-5. This action causes PNP transistor Q2 to conduct.

NOTE

Optical isolator U11 is dormant at this time, due to the high being applied at U11-2.

As shown in Figure 7-5, Q2 is connected in a common-base configuration (that is, its base is biased through resistors R16 and R17 from the positive and negative 62.5 Vdc supplies). When the internal transistor in U10 conducts, the emitter of Q2 is returned to +62.5 Vdc. Current flows from its collector towards the base of NPN transistor Q4, raising its base relative to its emitter. (The Q4 emitter is connected to −62.5 Vdc.) Q4 conducts to saturation sinking current through the load.

Exactly the opposite operation occurs in Driver B. When the signal applied to the drivers (from J1-13) is low, corresponding to Mark data present, Driver B is the active driver. The signal is double-inverted by inverters U9-5-6 and U6-14-15, and the resulting low is applied to optical isolator U11 (U11-2). An internal diode, connected across U11-1-2, conducts, turning on (or saturating) an internal transistor connected across U11-45.

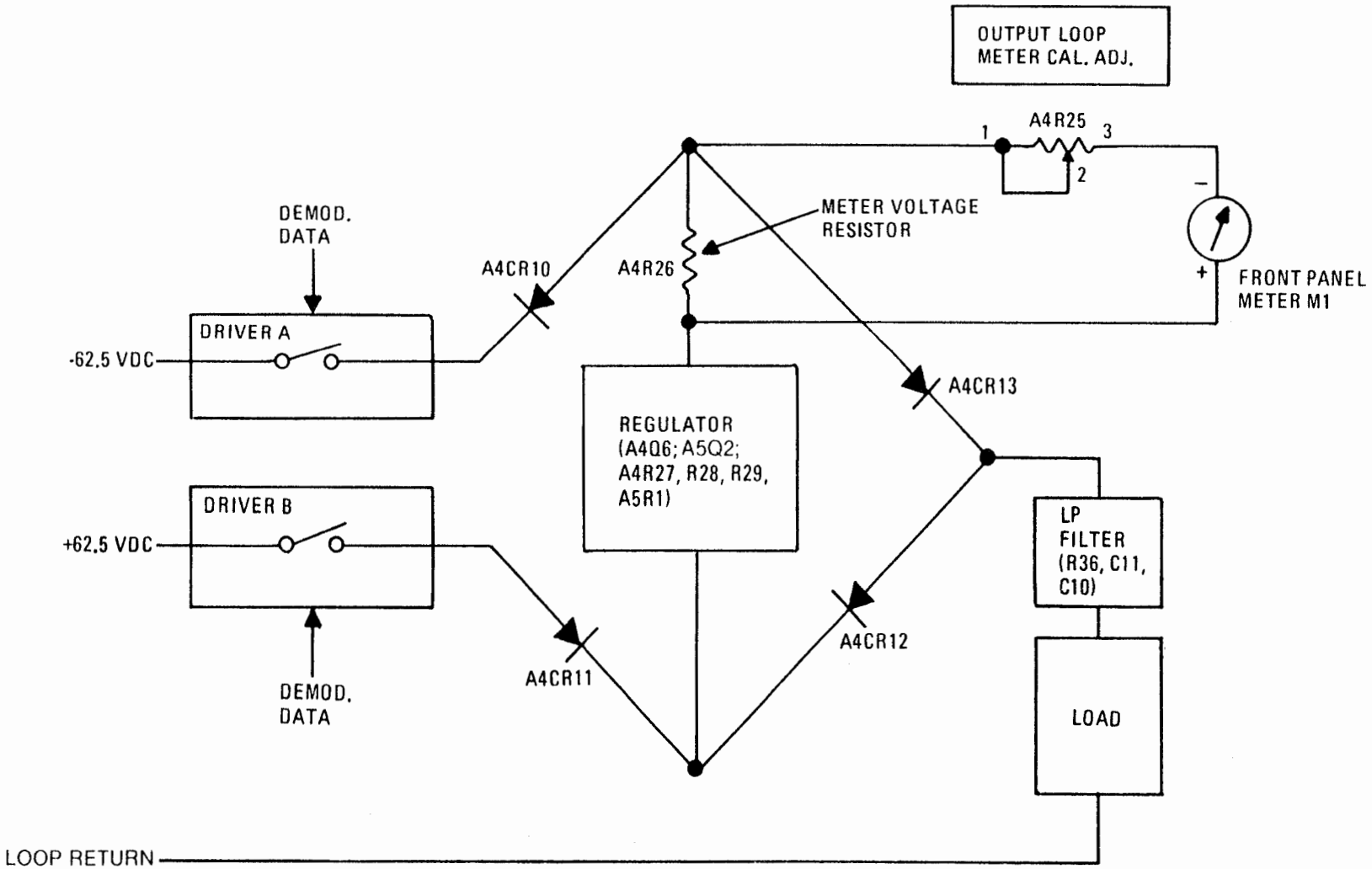


Figure 4-B. Interface PWB A4

Figure 4-11. Interface Pwb A4 Output Loop Driver Circuitry

NOTE

The double-inversion at the input of optical isolator U11 allows Drivers A and B to operate in a mutually-exclusive mode.

This action causes NPN transistor Q3 to conduct.

NOTE

Optical isolator U10 is dormant at this time, due to the high being applied at U10-2.

When Q3 conducts, its emitter is brought low. (The base of Q3 is biased through resistors R21 and R22 in the same way as PNP transistor Q2 of Driver A, but in a dual mode; Q2's base is brought to −62.5 Vdc through R16; Q3's base is brought to +62.5 Vdc through R21.) Collector current drawn by Q3 causes the base of Q5 to become negative with respect to the emitter. Q5 conducts to saturation, supplying current through the load.

4.4.4.8 Output Loop Current Regulator Operation

Refer to Figure 4-11. Drivers A and B (shown as switches) feed a special diode bridge that has one of its junctions (CR10 and Cr11) opened. Like the input loop circuit (Figure 4-10), a regulator and meter drive circuit is shown. The loading is connected across the "battery supply" (junction of CR13 and CR12) and is completely isolated with respect to the unit's ground. The lowpass filter shown retains load isolation, and also reduces inductive spikes coming back from the load.

Refer to Figure 7-5. Catching diodes CR8 and CR9, connected to the collectors of transistors Q4 and Q5, respectively, ensure that the voltage on the collectors never goes higher than the 62.5 Vdc supply voltages. This situation can sometimes occur due to the inductive spikes associated with the load.

Diodes CR6 and CR7 are included to protect the drivers in the event that the "battery supplies" are inadvertently connected backwards.

4.4.4.9 Equipment Interconnection - Theoretical Aspects

The data convention associated with the equipment is that a Low equals a Mark Condition and a high equals a Space Condition. In Neutral Mode, a Mark Condition is associated with a current condition at the TTY.

NOTE

Positive current flow is assumed, that is, current flows from a point of higher potential to a point of lower potential.

If a low is applied to Driver A and B, Driver B will be active and Driver A will be inactive, as described earlier. As shown in Figure 4-11, and detailed in Figure 7-5, Driver B is, in effect, a switch connected to the +62.5 Vdc supply. Since a Mark Condition implies current flow, the TTY load should be returned to −62.5 Vdc.

In Polar Mode, both Driver A and B will be active. The load will be returned to the common of the two 62.5 Vdc supplies.

Assuming that data processing is initiated with a Mark Condition (low), Driver B will be active and current will pass from the driver to the load. When data information goes to Space Condition (high), Driver A will be active and current will pass from the load to the driver.

From the preceding, it can be seen that the only hookup difference between Neutral and Polar Modes is the potential (relative to the positive or negative 62.5 Vdc loop supply) to which the TTY load is returned.

4.4.10 Conversion of CMOS Internal Outputs to RS-232 Outputs

Certain internal signals have to be converted from CMOS back to RS-232 representation. These are: Data Set Ready (to J1-9), indicating to the data terminal that the communications equipment is ready; Clear-To-Send (CTS-to-J1-10), that is routed back to the data terminal after a prescribed delay (that is, the delay between Request-To-Send and Clear-To-Send); Received Input Signal Detect (to J1-15), telling the data terminal that valid data is present; and Received Data (to J1-14).

Refer to Line Driver U7 in Figure 7-5. This driver was designed to convert TTL outputs to RS-232. Correspondingly, the maximum input voltage is specified to be + 7 volts. Since the logic levels used in this equipment are 0 volts and 12 volts, series diodes CR1, CR2 and CR3 are placed in series with the inputs to block excessive positive voltage levels. Current sinking, compatible with TTL requirements, is provided by Buffer/Inverter U6-7-6, U6-5-4 and U6-3-2.

CMOS logic levels applied at J1-13, J1-12 and J1-11 emerge as RS-232 logic levels at J1-14, J1-15 and J1-10, respectively. High CMOS levels convert to negative RS-232 levels. Since input U7-2 is provided, the Data Set Ready output at J1-P is positive whenever the modem is powered on.

The power to U7 is brought in through pass diodes CR4 (+ 12 Vdc) and CR5 (− 12 Vdc). These diodes are included to isolate the low impedance of the power supply from the U7 impedance, as recommended by the manufacturer.

Filter capacitors C3 and C6 are included to comply with RS-232 rise and fall time requirements.

4.4.4.11 Auto Start Relay Components

PNP transistor Q7 is the relay driver for the auto-start relay. When it is desired to close the relay, the auto start drive line is low (ASDL). When this condition occurs, Q7 conducts, closing the relay. Components R32 and CR14 negate relay kickback. Closing AS OVERRIDE switch S3 places a short across Q7, causing the relay to close independent of Q7.

4.4.5 TRANSISTOR/REGULATOR PWB ASSEMBLY A5 DESCRIPTION

Transistor/Regulator Pwb A5 contains components whose functions are related to other areas of the terminal, but whose heat sinking requirements require a remote mounting (except for NORM/LOOPBACK switch A5S1/1S3). The function of transistors Q1 and Q2 and their associated components is described in paragraph 4.4.4. The function of voltage regulators VR1 and VR2 and their associated components is described in paragraph 4.4.8. NORM/LOOPBACK switch A5S1/1S3 allows for various routings of the audio input and output signals during operation and equipment testing. Refer to Figure 7-6 for the schematic diagram of this pwb.

4.4.6 CONTROL AND INDICATOR PWB ASSEMBLY A6 DESCRIPTION

Control and Indicator Pwb A6 contains the transmit, receive and keyline sensing switches and status indicators. The function of these components is described where they apply in other parts of this section. The pwb also contains the driver circuit components for the receive status indicators. Refer to Figure 7-7 for a schematic diagram of this pwb.

4.4.7 FREQUENCY CONTROL BOARD ASSEMBLY A7 DESCRIPTION

Frequency Control Board Assembly A7 facilitates mounting of the front panel center and shift frequency selector switches. The function of the switches is described in paragraph 4.4.3. Refer to Figure 7-8 for wiring and functional information that applies to these switches.

4.4.8 POWER SUPPLY PWB ASSEMBLY PS7

Refer to Figures 7-9. A 48 Vrms input is applied to Diode Pack U1, whose output is filtered by components C1, C2, R1 and R2 to provide +62.5 Vdc and −62.5 Vdc outputs. A 19.5 Vrms input is applied to Diode Pack U1, whose output is filtered by components C3 and C4 to provide +12 Vdc and −12 Vdc unregulated outputs.

Refer to Figure 7-6. The +12 Vdc and −12 Vdc unregulated outputs are routed to Transistor/Regulator Pwb A5. Part of the −12 Vdc unregulated voltage is routed straight through the pwb to provide relay drive voltage. The remaining portion of the −12 Vdc input and all of the +12 Vdc input to the pwb are applied to Voltage Regulators VR1 and VR2, which provide regulated outputs of −12 Vdc and +12 Vdc, respectively.

4.4.9 INTERCONNECTION PWB ASSEMBLY W1 DESCRIPTION

Interconnection Pwb W1 contains the trace wiring and interconnection receptacles that facilitate signal routing and wiring of the terminal's pwb's and other components. Refer to Figure 7-10 for specific information.

4.4.10 WIRING ASSEMBLIES W2 THROUGH W4 DETAILS

Detail information applicable to the Chassis and Panel Wiring Assembly W2 and chassis/panel components, RS-232 Interface Wiring Assembly W3, and Low Level Wiring Assembly W4 are shown in Figure 7-2.

SECTION 5

MAINTENANCE

5.1 INTRODUCTION

This section covers the maintenance instructions for the RF-3352 FSK Terminal. Included herein are disassembly and removal instructions, troubleshooting instructions, and various technical aids and references to assist the technician in maintaining the terminal.

5.2 TROUBLESHOOTING AND PERFORMANCE VERIFICATION

In the event that trouble develops in the terminal, first identify the apparent source and then refer to the applicable schematic diagram(s) and component location diagram(s) of Sections 7 and 6, respectively. (Section 7 also contains a tabular listing of all connectors, pins, switches, controls, and test points and their functional identifications in the terminal.) As technical aids, this section contains a series of Test Point Typical Data Sheets, that show the typical test data that should be measured at each test point, and a terminal dc voltage source diagram for power supply voltage checking and reference to the descriptions and analyses of Section 4 is also recommended.

5.3 RECOMMENDED TEST EQUIPMENT

The following test equipment, or its technical equivalent, is recommended for performing tests of the terminal.

a. VOM (Volt-Ohmmeter) - Simpson Model 260

b. Oscilloscope - Tektronix Model 465

c. RMS Voltmeter - Hewlett & Packard Model HP-400F

5.4 REMOVAL OF MODULATOR PWB ASSEMBLY A1

a. Refer to Figure 5-1. Place a flat blade screwdriver through the access holes in the side of the Chassis (8) and loosen the four Retaining Screws (37).

b. Lift Demodulator Pwb A2 (17) up and towards the rear of Chassis (8) to gain access to Modulator Pwb A1 (36).

c. Use a Philips-head screwdriver to loosen and remove the nine No. 4-40 Screws, No. 4 Lockwashers, and No. 4 Flatwashers (35).

d. Carefully separate Modulator Pwb A1 (36), and its stiffener, from Interconnector Pwb W1 (19).

5.5 REMOVAL OF DEMODULATOR PWB ASSEMBLY A2

a. Refer to Figure 5-1. Remove Cable Connector A2W1P1 (11) from Pwb Connector W1XA2 (12).

b. Use a Philips-head screwdriver to loosen and remove the 15 No. 4-40 Screws, No. 4 Lockwashers, and No. 4 Flatwashers (15).

c. Carefully separate Demodulator Pwb A2 (17) from Hinged Demodulator Frame (13).

5.6 REMOVAL OF TIMING AND CONTROL PWB ASSEMBLY A3

a. Refer to Figure 5-1. Use a Philips-head screwdriver to loosen and remove the five No. 4-40 Screws, No. 4 Lockwashers, and No. 4 Flatwashers (32).

b. Carefully separate Timing and Control Pwb A3 (33) and its stiffener from Interconnection Pwb W1 (19).

5.7 REMOVAL OF INTERFACE PWB ASSEMBLY A4

a. Refer to Figure 5-1. Use a Philips-head screwdriver to loosen and remove the five No. 4-40 Screws, No. 4 Lockwashers, and No. 4 Flatwashers (9).

b. Carefully separate Interface Pwb A4 (10) and its stiffener from Interconnection Pwb W1 (19).

5.8 REMOVAL OF TRANSISTOR/REGULATOR PWB ASSEMBLY A5

a. Refer to Figure 5-1. Remove Cable Connector W2P5 (4) from Pwb Connector A5J2 (5).

b. Use a Philips-head screwdriver to loosen and remove the three No. 6-32 Screws that secure the Transistor/Regulator Pwb A5 (6) to the Chassis (8).

c. Loosen and remove the two No. 4-40 Screws, No. 4 Lockwashers, and No. 4 Flatwashers (7).

d. Carefully separate Transistor/Regulator Pwb A5 (6) and its stiffener from Chassis (8) and Interconnection Pwb W1 (19).

5.9 REMOVAL OF POWER SUPPLY PWB ASSEMBLY PS1

a. Refer to Figure 5-1. Remove Cable Connector W2P1 (22) from Pwb Connector PS1J6 (23).

b. Use a Philips-head screwdriver to loosen and remove the four No. 4-40 Screws, No. 4 Lockwashers and No. 4 Flatwashers (26).

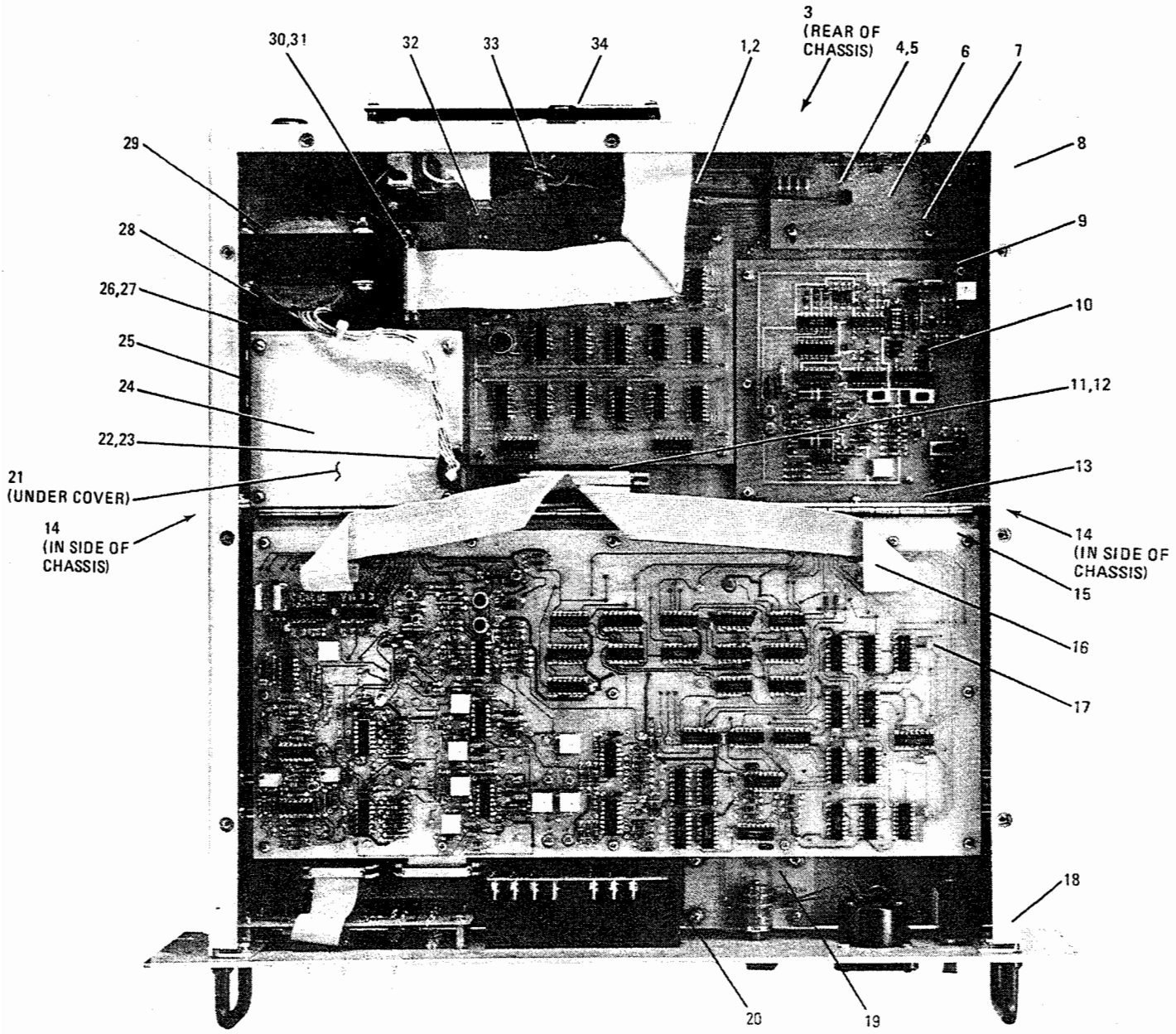


Figure 5-1. RF-3352 FSK Terminal Disassembly Details (Sheet 1 of 3)

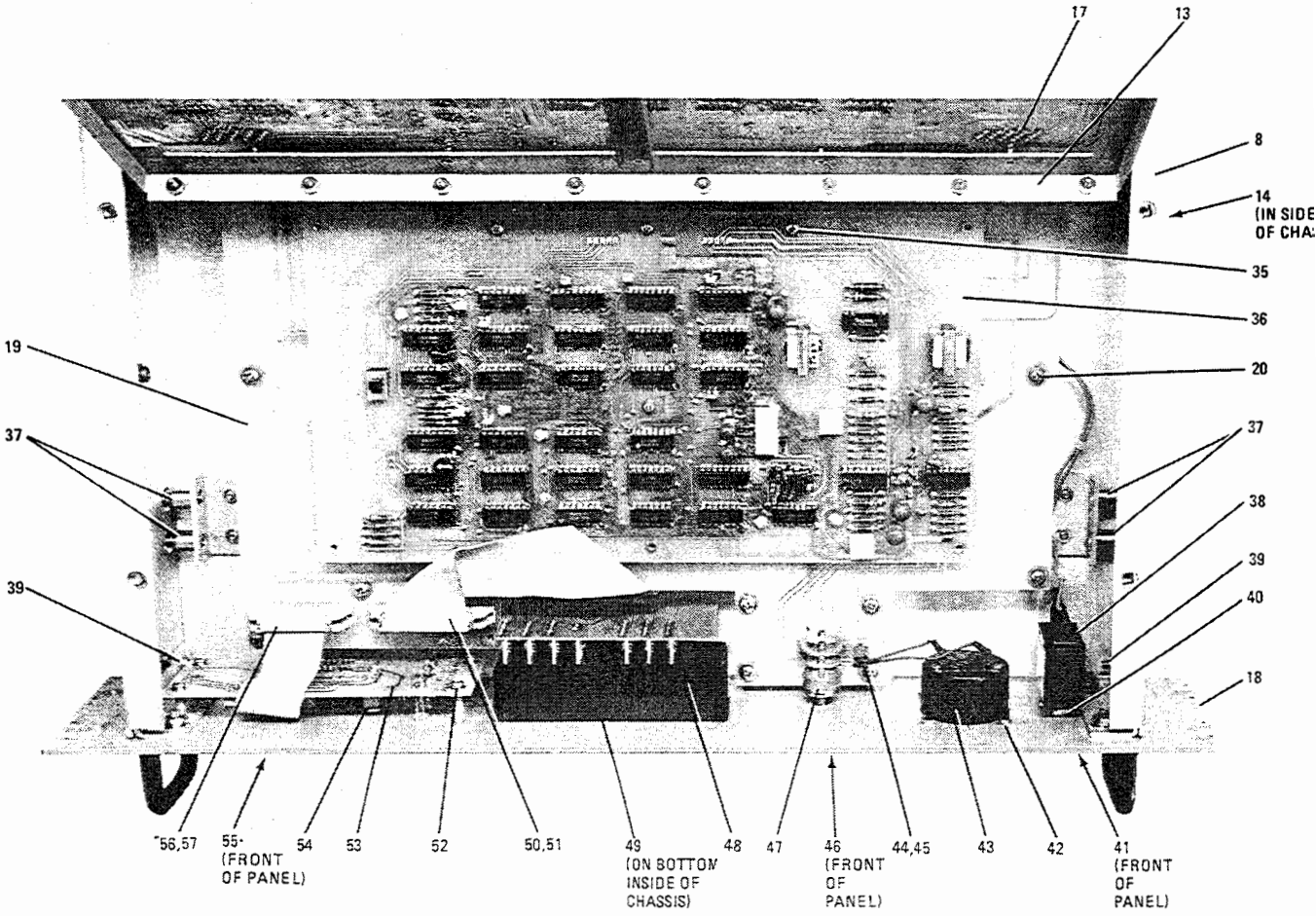


Figure 5-1. RF-3352 FSK Terminal Disassembly Details (Sheet 2 of 3)

LEGEND FOR FIGURE 5-1

1. Cable Connector W14P4
2. Pwb Connector W1J2
3. Screws (3 used)
4. Cable Connector W2P5
5. Pwb Connector A5J2
6. Transistor/Regulator Pwb A5
7. Screws, Lockwashers, Flatwashers (2 used)
8. Chassis
9. Screws, Lockwashers, Flatwashers (5 used)
10. Interface Pwb A4
11. Cable Connector A2W1P1
12. Pwb Connector W1XA2
13. Hinged Demodulator Frame
14. Screws, Lockwashers, Flatwashers, Hex Nut (4 used)
15. Screws, Lockwashers, Flatwashers (15 used)
16. Demodulator Cable A2W1
17. Demodulator Pwb A2
18. Front Panel Assembly
19. Interconnection Pwb W1
20. Screws, Lockwashers, Flatwashers (19 used)
21. Screw, Lockwasher, Flatwasher
22. Cable Connector W2P1
23. Pwb Connector PS1J6
24. Cover
25. Power Supply Pwb PS1
26. Screws, Lockwashers, Flatwashers (4 used)
27. Standoffs (4 used)
28. Hex Nuts, Lockwashers, Flatwashers, Screws (4 used)
29. Transformer 1T1
30. Cable Connector W3P3
31. Pwb Connector W1J3
32. Screws, Lockwashers, Flatwashers (5 used)
33. Timing and Control Pwb A3
34. Connector 1J5
35. Screws, Lockwashers, Flatwashers (9 used)
36. Modulator Pwb A1
37. Retaining Screws (4 used)
38. Circuit Breaker 1CB1
39. Screws (4 used)
40. Inside Hex Nut
41. Outside Hex Nut
42. Hex Nuts, Lockwashers, Screws
43. Meter 1M1
44. Cable Connector W2P2
45. Pwb Connector W1J6
46. Knob
47. Selector Switch W1S1
48. Frequency Control Board A7
49. Screws (2 used)
50. Cable Connector A7W1P1
51. Pwb Connector W1J5
52. Screws, Lockwashers, Flatwashers (4 used)
53. Control and Indicator Pwb A6
54. Inside Hex Nuts (3 used)
55. Outside Hex Nuts (3 used)
56. Cable Connector A6W1P1
57. Pwb Connector W1J4

Figure 5-1. RF-3352 FSK Terminal Disassembly Details
(Sheet 3 of 3)

c. Remove Cover (24).

d. Remove the four standoffs (27) and, using a Philips-head screwdriver, loosen and remove No. 4-40 Screw, No. 4 Lockwasher, and No. 4 Flatwasher (21).

e. Carefully separate Power Supply Pwb PS1 (25) from Interconnection Pwb W1 (19).

5.10 REMOVAL OF TRANSFORMER 1T1

a. Refer to Figure 5-2. Unsolder or cut and tag Transformer 1T1 wires as directed therein.

b. Refer to Figure 5-2. Use a No. 10 Nut Driver and a flat blade screwdriver to loosen and remove the four No. 10-32 Hex Nuts, No. 10 Lockwashers, No. 10 Flatwashers, and No. 10-32 Screws (28).

c. Carefully remove Transformer 1T1 (29) from Chassis (8).

5.11 REMOVAL OF FRONT PANEL ASSEMBLY

a. Refer to Figure 5-1. Remove Cable Connector W2P2 (44) from Pwb Connector W1J6 (45), Cable Connector A7W1P1 (50) from Pwb Connector W1J5 (51), and Cable Connector A6W1P1 (56) from Pwb Connector W1J4 (57).

b. Remove Knob (46) from Selector Switch W1S1 (47).

c. Use a flatblade screwdriver to loosen and remove the four No. 8-32 Screws (39) and the two No. 6-32 Screws (49) that secure Front Panel Assembly (18) to the Chassis (8).

d. Carefully separate Front Panel Assembly (18) from the Chassis (8).

5.12 REMOVAL OF CONTROL AND INDICATOR PWB ASSEMBLY A6

a. Refer to Figure 5-1. Remove Front Panel Assembly (18) as described in Paragraph 5-11.

b. Loosen the three Inside Hex Nuts (54).

c. Use a Philips-head screwdriver to loosen and remove the four No. 4-40 Screws, No. 4 Lockwashers, and No. 4 Flatwashers (52).

d. Remove the three Outside Hex Nuts (55), using a nut driver.

e. Carefully separate Control and Indicator Pwb A6 (53) from Front Panel Assembly (18).

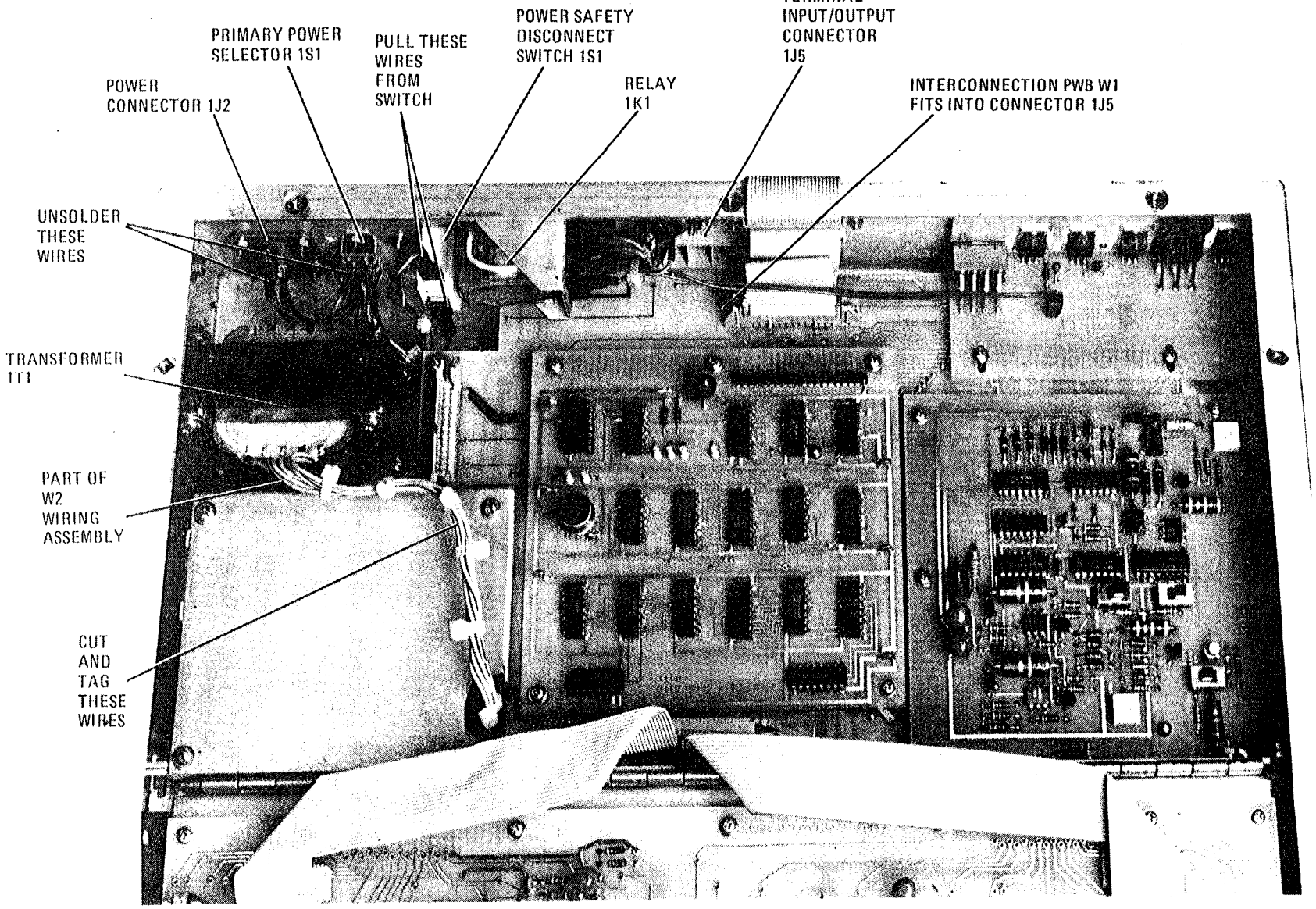


Figure 5-2. RF-3352 FSK Terminal - Transformer 1T1 and Inside Rear Panel Component Replacement Details

5.13 REMOVAL OF FREQUENCY CONTROL BOARD ASSEMBLY A7

a. Refer to Figure 5-1. Remove Front Panel Assembly (18) as described in Paragraph 5-11.

b. Press plastic casing of Frequency Control Board Assembly A7 (48) inward (towards assembly's center) and push assembly out of Front Panel Assembly (18).

5.14 REMOVAL OF METER 1M1 AND CIRCUIT BREAKER 1CB1

a. Refer to Figure 5-1. Use a flat blade screwdriver to loosen and remove the four meter screws, hex nuts, and lockwashers (42).

b. Carefully push Meter 1M1 (43) and its gasket out of Front Panel Assembly (18).

c. Loosen Inside Hex Nut (40), then remove Outside Hex Nut (41).

d. Pull Circuit Breaker 1CB1 out of the Front Panel Assembly (18).

5.15 REMOVAL OF INTERCONNECTION PWB ASSEMBLY W1

a. Refer to Figure 5-1. Remove Cable Connector A2W1P1 (11) from Pwb Connector W1XA2, Cable Connector W3P3 (30) from Pwb Connector W1J3 (31), and Cable Connector W4P4 (1) from Pwb Connector W1J2 (2).

b. Place a flatblade screwdriver through the access holes in each side of Chassis (8) and loosen the four Retaining Screws (37).

c. Lift Demodulator Pwb A2 (17) up and towards rear of Chassis (8).

d. Use a flatblade screwdriver to loosen and remove the four No. 6-32 Screws, No. 6 Lockwashers, No. 6 Flatwashers, and No. 6-32 Hex Nuts (14) that secure Hinged Demodulator Frame (13) to Chassis (8).

e. Carefully separate Demodulator and Frame Assembly (13 and 17) from Chassis (8).

f. Separate Front Panel Assembly (18) from Chassis (8) as described in Paragraph 11.

g. Separate Modulator Pwb A1 (36), Timing and Control Pwb A3 (33), Interface Pwb A4 (10), Transistor/Regulator Pwb A5 (6), and Power Supply Pwb PS1 (25) from Interconnection Pwb W1 (19) as described in Paragraphs 5-4, 5-6, 5-7, 5-8, and 5-9, respectively.

h. Use a Philips-head screwdriver to loosen and remove the 19 No. 6 Screws, No. 6 Lockwashers and No. 6 Flatwashers (20) that secure Interconnection Pwb W1 (19) to Chassis (8).

i. Carefully separate Interconnection Pwb W1 (19) from Chassis (8).

NOTE

When removing Interconnection Pwb W1 (19), move Pwb towards front of Chassis (8) and out of inside surface of Terminal Input/Output Connector 1J5 (see Figure 5-1 and 5-2).

5.16 PWB REPLACEMENT - SPECIAL INSTRUCTIONS

When replacing Modulator Pwb A1, Timing and Control Pwb A3, Interface Pwb A4, Transistor/Regulator Pwb A5, and Power Supply Pwb PS1, careful alignment of their connector pins is mandatory.

CAUTION

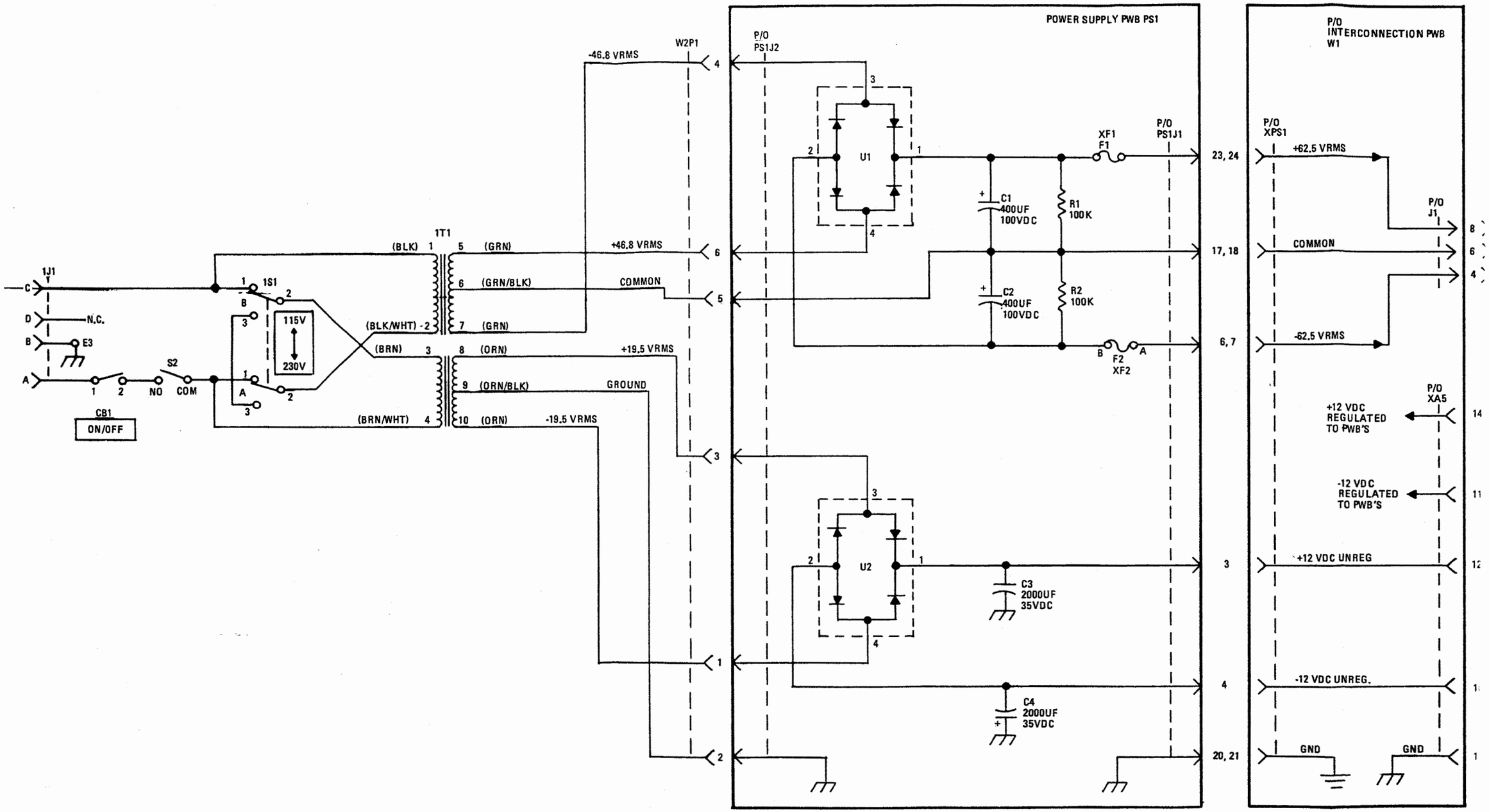
The connector pin contacts are very fragile. When installing the pwb, avoid excessive bending of the board, and remember to replace the applicable board stiffeners.

5.17 RF-3352 FSK TERMINAL VOLTAGE SOURCE DIAGRAM

Figure 5-3 shows the ac and dc voltage source and distribution data in the terminal. Refer to the applicable schematic diagrams of Section 7 for voltage distribution within the various pwb's.

5.18 RF - 3352 FSK TERMINAL ADJUSTMENT°, CONTROL, AND TEST POINT LOCATIONS

Figure 5-4 shows the locations of all terminal assembly and adjustment, control, and test point locations


1J1
C
D
N.C.
B
E3
A
S2
1
2
NO
COM
CB1
ON/OFF
1S1
B
A
115V
230V
1T1
(BLK) 1
5 (GRN)
6 (GRN/BLK)
(BLK/WHT) -2
7 (GRN)
(BRN) 3
8 (ORN)
9 (ORN/BLK)
(BRN/WHT) 4
10 (ORN)
-46.8 VRMS
+46.8 VRMS
COMMON
+19.5 VRMS
GROUND
-19.5 VRMS
W2P1
4
6
5
3
1
2
POWER SUPPLY PWB PS1
P/O
PS1J2
U1
U2
C1
400UF
100VDC
C2
400UF
100VDC
C3
2000UF
35VDC
C4
2000UF
35VDC
R1
100K
R2
100K
XF1
F1
XF2
F2
P/O
PS1J1
23, 24
17, 18
6, 7
3
4
20, 21
P/O
INTERCONNECTION PWB
W1
P/O
XPS1
+62.5 VRMS
COMMON
-62.5 VRMS
P/O
J1
8
6
4
P/O
XA5
+12 VDC
REGULATED
TO PWB'S
14
-12 VDC
REGULATED
TO PWB'S
11
+12 VDC UNREG
12
-12 VDC UNREG.
GND
GND

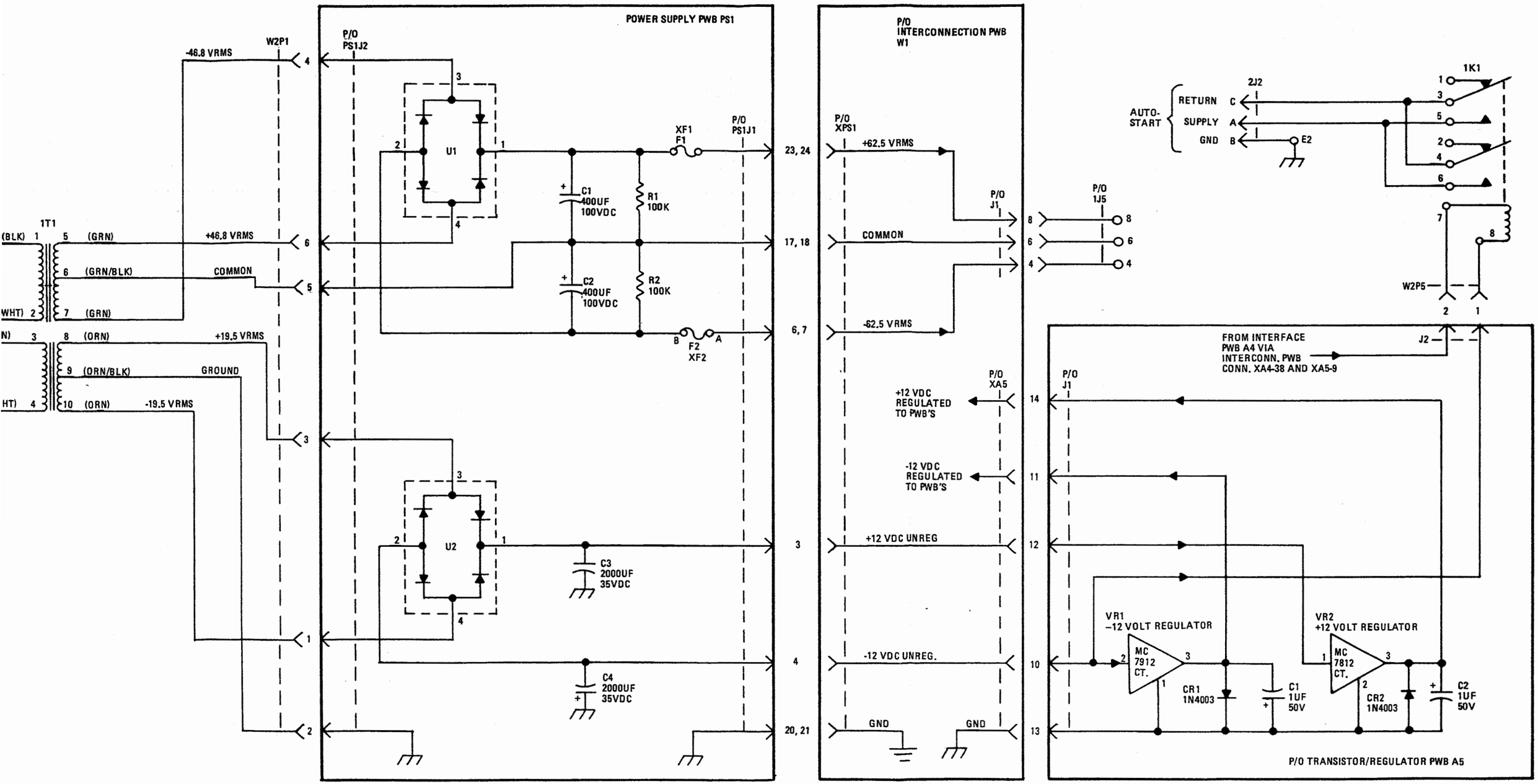
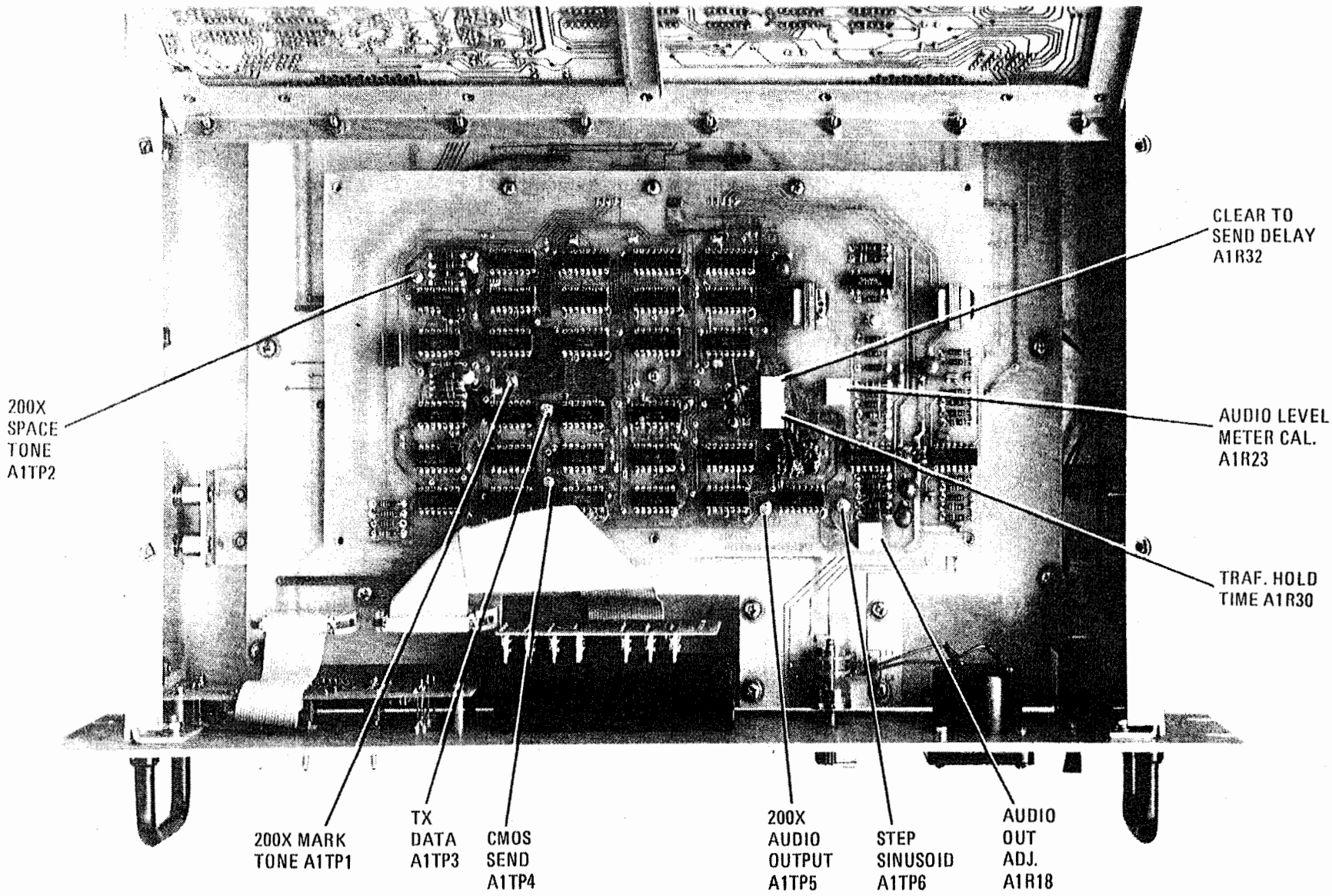


Figure 5-3. RF-3352 FSK Terminal Voltage Source Diagram



MODULATOR PWB ASSEMBLY A1 ADJUSTMENTS, CONTROLS, AND TEST POINTS

Figure 5-4. RF - 3352 FSK Terminal - Assembly Adjustment, Control, and Test Point Locations (Sheet 1 of 3)

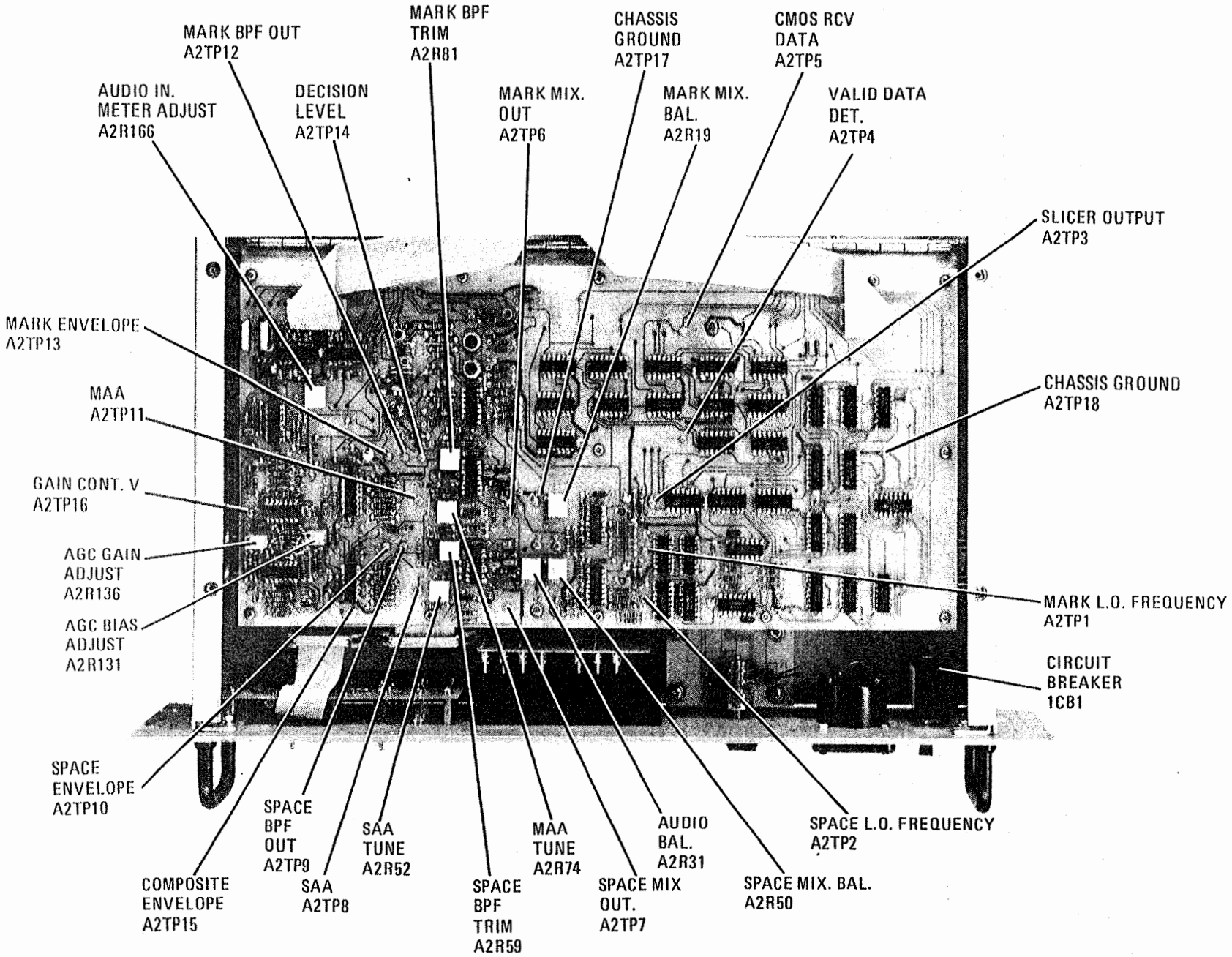
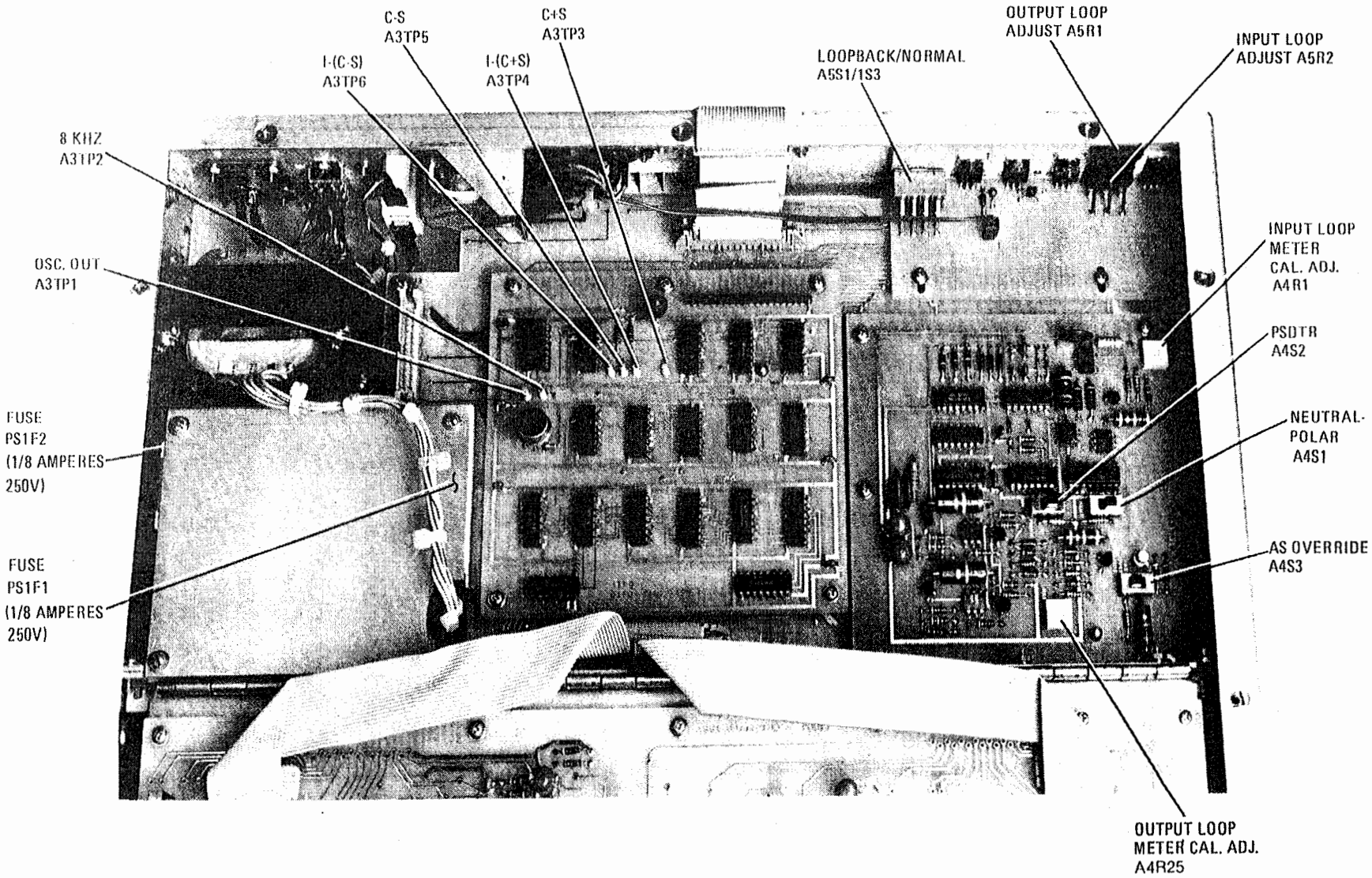


Figure 5-4. RF-3352 FSK Terminal - Assembly Adjustment, Control, and Test Point Locations (Sheet 2 of 3)

DEMODULATOR PWB ASSEMBLY A2 ADJUSTMENTS, CONTROLS, AND TEST POINTS



TIMING AND CONTROL PWB ASSEMBLY A3, INTERFACE PWB ASSEMBLY A4, AND TRANSISTOR/ REGULATOR PWB ASSEMBLY A5
ADJUSTMENTS, CONTROLS, AND TEST POINTS

Figure 5-4. RF - 3352 FSK Terminal - Assembly Adjustment, Control, and Test Point Locations (Sheet 3 of 3)

5.19 TEST POINT TYPICAL DATA TABLES

Tables 5-1 through 5-32 comprise waveforms and test data measured at the applicable test points of a normally operating RF-3352 FSK Terminal. Test conditions, control positions, and interpretive data are given.

5.20 RF-3352 FSK TERMINAL ALIGNMENT PROCEDURES

Complete alignment procedures for the RF-3352 FSK Terminal are described in subsequenc paragraphs 5.20.1 through 5.20.4. For reference the following procedures are included, in the sequence given.

5.20.1 Through 5.20.4 For reference the following procedures are included, in the sequence given.

a. Modulator Pwb Assembly A1 Alignment Procedures - Paragraph 5.20.1

   1. Audio Output Level Adjustment and Meter (Audio Out) Calibration - 5.20.1.a.

   2. Traffic Detector and Clear-to-Send Delay Adjustments - 5.20.1.6.

b. Demodulator Pwb Assembly A2 Alignment Procedcures - 5.20.2.

   1. Mark and Space Mixers Balance Adjustment - 5.20.2.a.

   2. AGC Adjustment - 5.20.2.b.

   3. Bandpass Filter Adjustment - 5.20.2.c.

   4. Mark and Space Balance Adjustment - 5.20.2.d.

   5. Input Level Meter (Audio In) Adjustment - 5.20.2.e.

c. Alignment Procedures - Timing and Control Pwb A3, Transistor/Regulator Pwb A5, Control and Indicator Pwb A6, Frequency Control Board A7, and Power Supply Pwb PS1-5.20.3.

d. Interface Pwb Assembly A4 Alignment Procedures - 5.20.4.

   1. Output Loop and Loop Out Meter Adjustment - 5.20.4.a.

   2. Input Loop and Input Loop Meter Adjustment (TTY Not In Loop) - 5.20.4.6.

   3. Input Loop and Loop In Meter Adjustment (TTY Mode) - 5.20.4.c.

5.20.1 Modulator Pwb Assembly A1 Alignment Procedures.

a. Audio Output Level Adjustment and Meter (Audio Out) Calibration.

   1. Refer to Figure 3-1. Place TRANSMIT-SENSE NORM/REV/OFF Switch A6S2 in NORM position, TRANSMIT-KEYLINE CLOSED/OPEN/AUTO Switch A6S1 in AUTO position, adjust the TONE SELECTION (HZ) Switches A7S1 to provide a frequency of 1500 $\pm$000 Hz.

   2. Refer to Figure 3-2. Place LOOPBACK/NORM Switch 1S3/A5S1 in LOOP-BACK position.

   3. Refer to Figure 5-4 (Sheet 1 of 3). Place IDLE SELECT Switch A1S1 in M position.

4. Refer to Figures 6-2 and 7-2. Attach an RMS Voltmeter (Hewlett Packard Model HP-400F, or equivalent) to Pins 4 and 6 of transformer T2.

5. Refer to Figure 5-4 (Sheet 1 of 3). Adjust AUDIO OUT ADJ. Control A1R18 to obtain a 0dBm indication at the voltmeter.

6. Place front panel METER FUNCTION SELECTOR W1S1 in AUDIO OUT position.

7. Adjust AUDIO LEVEL METER CAL. Control A1R32 to obtain 0dBm indication at front panel FUNCTION DISPLAY Meter 1M1.

NOTE

If a 0 dBm audio level is not desired, readjust AUDIO OUT ADJ Control A1R18 to desired level.

b. Traffic Detector and Clear-to-Send Delay Adjustments.

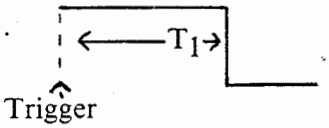
1. Remove Interface Pwb Assembly A4 as described in Paragraph 5.7.

2. Refer to Figure 3-1. Place TRANSMIT-KEYLINE CLOSED/OPEN/AUTO Switch A6S1 in AUTO position and TRANSMIT-SENSE NORM/REV/OFF Switch A6S2 to NORM position.

3. Refer to Figures 6-2 and 7-2. Connect +12 Vdc to U2-11 and connect a jumper between U20-7 and CMOS SEND Test Point TP4. Connect another jumper between U19-12 and TX data Test Point TP3.

4. Connect an oscilloscope (Tektronix Model 464 or equivalent) to U20-9. Trigger oscilloscope in normal mode on the positive-going transition of the waveform observed.

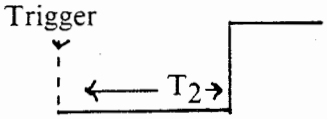
5. Refer to Figure 5-4 (Sheet 1 of 3). Adjust TRAF. HOLD TIME, Control A1R30 for the desired traffic detector delay time. The time relationship is shown below:



T_1 = 400 - 2500 Milliseconds (T_1 has been factory-set to 1000 Milliseconds.)

6. Trigger oscilloscope on the negative-going transition of the waveform.

7. Adjust CLEAR-TO-SEND DELAY Control A1R32 for the desired clear-to-send delay time. The time relationship is shown below:



T_2 = 100 - 2500 Milliseconds (T_2 has been factory-set to 1000 Milliseconds)

8. Remove +12 Vdc, jumpers, and oscilloscope. Replace Interface Pwb Assembly A4 and reset terminal controls for manual operation.

5.20.2 Demodulator Pwb Assembly A2 Alignment Procedures.

a. Mark and Space Mixers Balance Adjustment.

NOTE

This procedure must be performed whenever the Demodulator Pwb Assembly A2 has been replaced.

1. Refer to Figures 3-1 and 3-2. Place TRANSMIT-SENSE NORM/REV/OFF Switch A6S2 in OFF position and LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

2. Refer to Figure 5-4 (Sheet 2 of 3). Attach an oscilloscope (Tektronix Model 465,
or equivalent) to MARK MIX. OUT Test Point A27P6.

3. Adjust MARK MIX. BAL. Control A2R19 for a minimum peak-to-peak signal (approximately 20 mV).

4. Reconnect oscilloscope to SPACE MIX. OUT Test Point A27P7 and adjust SPACE MIX. BAL. Control A2R50 for a minimum peak-to-peak signal (approximately 20 mV).

5. Disconnect oscilloscope and reset terminal controls for normal operation.

b. AGC Adjustment.

NOTE

This procedure must be performed whenever the Demodulator Pwb Assembly A2 has been replaced, or when any component of the AGC Amplifier/Scaler Circuit has been replaced.

1. Refer to Figures 3-1 and 3-2. Place TRANSMIT-KEYLINE CLOSED/OPEN/AUTO Switch A6S1 in AUTO position; TRANSMIT-SENSE NORM/REV/OFF
Switch A6S2 in NORM Position, RECEIVE-SENSE NORM/MARK HOLD/REV Switch A6S3 in NORM position, set TONE SELECTION (Hz) Switches A7S1 to provide a frequency of 1500 ±085 Hz, and place LOOP-BACK/NORM
Switch 1S3/A5S1 Switch in LOOPBACK position.

2. Apply 1 : 1 Mark/Space data to the terminal.

NOTE

Mark/Space data, at a Baud Rate of 62.5, may be simulated as follows: Remove the Interface Pwb Assembly A4, as described in Paragraph 5.7. On Modulator Pwb Assembly A1, connect a jumper between U17-1 and TX DATA Test Point A17P3. (Refer to Figures 7-2 and 5-4 [Sheet 1 of 3] for location information.)

3. Refer to Figures 6-3 and 7-3. Connect an RMS Voltmeter (Hewlett-Packard Model HP-400F, or equivalent) between Pins 1 and 3 of transformer T1.

4. Refer to Figure 5-4 (Sheet 1 of 3). Adjust AUDIO OUT ADJ. Control A1R18 to obtain a -30 dBm indication at the rms voltmeter.

5. Refer to Figure 7-3. Connect a voltohmmeter (Simpson Model 260, or equivalent) to the cathode of diode CR13.

6. Refer to Figure 5-4 (Sheet 2 of 3). Adjust AGC bias adjust Control A2R131 to obtain a 0 Vdc indication at the voltohmmeter.

7. Adjust AUDIO OUT ADJ. Control A1R18 to obtain a 0 dBm indication at the rms voltmeter.

8. Refer to Figure 5-4 (Sheet 2 of 3). Adjust AGC GAIN ADJUST Control A2R136 to obtain a +6 Vdc indication at the voltohmmeter.

9. Repeat steps b.4 through b.8 until no further improvement in the measurements required can be obtained.

NOTE

Subsequent step b.10 through b-12 need only be performed if transistor A2Q3 has been replaced.

10. Connect the voltohmmeter to the anode of diode CR13.

11. Adjust AUDIO OUT ADJ. Control A1R18 to obtain a +3 Vdc indication at the voltohmmeter.

12. Check and make certain that the signal level across Pins 1 and 3 of transformer T1 is between -10 dBm and -12 dBm, as indicated on the rms voltohmmeter.

13. Disconnect test equipment. Reset terminal controls for normal operation.

c. Bandpass Filter Adjustment.

1. Refer to Figures 3-1 and 3-2. Place TRANSMIT-SENSE NORM/REV/OFF Switch A6S2 in NORM position, LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position, and adjust TONE SELECTION (Hz) Switches A7S1 to provide a frequency of 1500 ±0000 Hz.

2. Refer to Figure 5-4 (Sheet 1 of 3). Place IDLE SELECT Switch A1S1 in M position.

3. Connect a jumper between GAIN CONT. V Test Point A2TP16 and CHASSIS GROUND Test Point A2TP17.

4. Connect a voltohmmeter (Simpson Model 260, or equivalent) to MARK BPF OUT Test Point A2TP12.

5. Adjust MAA TUNE Control A2R74 and MARK BPF TRIM. Control A2R81 to obtain a peak indication at the voltohmmeter.

6. Connect the voltohmmeter to SPACE BPF OUT Test Point A27P9.

7. Adjust SAA TUNE Control A2R52 and SPACE BPF TRIM. Control A2R59 to obtain a peak indication at the voltohmmeter.

8. Remove voltohmmeter and jumper. Reset terminal controls for normal operation.

d. Mark and Space Balance Adjustment.

1. Refer to Figures 3-1 and 3-2. Place TRANSMIT-SENSE NORM/REV/OFF Switch A6S2 in NORM Position, LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position and adjust TONE SELECTION (Hz) Switches A7S1 to provide a frequency of 1500 ±085 Hz.

2. Refer to Figure 5-4 (Sheet 1 of 3). Place IDLE SELECT Switch A1S1 in M position.

3. Refer to Figure 5-4 (Sheet 2 of 3). Connect a voltohmmeter (Simpson Model 260, or equivalent) to VALID DATA DET. Test Point A2TP4.

4. Adjust AUDIO BAL. Control A2R31 to obtain 0 Vdc indication at the volt-ohmmeter.

5. Remove voltohmmeter and reset terminal controls for normal operation.

e. Input Level Meter (Audio In) Adjustment.

1. Refer to Figures 3-1 and 3-2. Place TRANSMIT-SENSE NORM/REV/OFF Switch A6S2 in NORM position, LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position, and adjust TONE SELECTION (Hz) Switches A7S1 to provide a frequency of 1500 ±085 Hz.

2. Refer to Figure 5-4 (Sheet 1 of 3). Place IDLE SELECT Switch A1S1 in M position.

3. Refer to Figures 6-3 and 7-3. Connect an RMS Voltmeter (Hewlett Packard Model HP-400F, or equivalent) across Pins 1 and 3 of transformer T1.

4. Refer to Figure 5-4 (Sheet 1 of 3). Adjust AUDIO OUT ADJ. Control A1R18 to obtain a 0dBm indication at the voltmeter.

5. Place front panel METER FUNCTION SELECTOR W1S1 in AUDIO IN position.

6. Refer to Figure 5-4 (Sheet 2 of 3). Adjust AUDIO IN. METER ADJUST Control A2R166 for 0dBm indication on front panel FUNCTION DISPLAY Meter 1R1.

7. Disconnect RMS Voltmeter and reset terminal controls for normal operation.

5.20.3 Alignment Procedures - Timing and Control Pwb A3, Transistor/Regulator Pwb A5, Control and Indicator Pwb A6, Frequency Control Board A7, and Power Supply Pwb P51.

No alignment procedures apply to Timing and Control Pwb A3, Control and Indicator Pwb A6, Frequency Control Board A7, and Power Supply Pwb P51. Alignment procedures applicable to the Transistor/Regulator Pwb A5 are included in the Interface Pwb A4 procedures of Paragraph 5.20.4.

5.20.4 Interface Pwb Assembly A4 Alignment Procedures.

a. Output Loop and Loop Out Meter Adjustment.

CAUTION

The connections described in subsequent steps a.1 through a.6 should be accomplished prior to applying power to any of the equipment described.

1. Connect the terminal for TTY operation.

NOTE

The terminal input and output must not be connected in Common Loop Mode. Also, if a TTY is not in the loop, complete the loop by substitutint a 100 ohm 2 watt resistor in its place.

2. Refer to Figure 3-2. Remove cover from INPUT/OUTPUT TERMINAL CONNECTOR 1J5.

3. Unscrew and disconnect terminal space lug connection to 1J5-9 (DATA OUT connection). Connect the common lead of a voltohmmeter (Simpson Model 260, or equivalent) to the disconnected terminal spade lug.

4. Connect the positive voltohmmeter lead to the 1J5-9 terminal connection.

5. Set the voltohmmeter to the 100MA range.

6. Refer to Figure 3-1. Place RECEIVE-SENSE NORM/MARK HOLD/REV Switch A6S3 in MARK HOLD position.

7. Apply power to the equipment. Refer to Figure 3-2.

NOTE

If connector plate is left off of 1J5, PRIMARY POWER DISCONNECT Switch 1S2 (Figure 3-2) will have to be jumpered or held depressed in order for primary power to be supplied to the terminal.

8. Adjust OUTPUT LOOP ADJUST Control A5R1 to supply the desired current, as indicated on the voltohmmeter.

9. Refer to Figure 3-1. Place METER FUNCTION SELECTOR W1S1 in LOOP OUT position.

10. Refer to Figure 5-4 (Sheet 3 of 3). Adjust OUTPUT LOOP METER CAL. ADJ. Control A4R25 until current indicated on front panel FUNCTION DISPLAY METER 1M1 is identical to that of the voltohmmeter.

11. Disconnect voltohmmeter from 1J5-9 and its mating spade lug. Reconnect spade lug to 1J5-9.

12. Replace cover on 1J5 and reset terminal controls for normal operation.

b. Input Loop and Input Loop Meter Adjustment (TTY Not In Loop).

CAUTION

The connectors described in subsequent steps b.1 through b.13 should be accomplished prior to applying power to any of the equipment described.

1. Refer to Figure 3-2. Remove cover from INPUT/OUTPUT TERMINAL CONNECTOR 1J5.

2. Unscrew and disconnect terminal spade lug connections to 1J5-2 and -3 (DATA IN Donnections). Connect the common lead of a voltohmmeter (Simpson Model 260, or equivalent) to 1J5-3.

3. Connect the positive voltohmmeter lead to the 1J5-7 terminal connection.

4. Connect a jumper between terminal connections 1J5-2 and 1J5-5.

5. Set the voltohmmeter to the 100 MA range.

6. Rotate INPUT LOOP ADJUST CONTROL A5R2 fully ccw.

7. Apply power to the equipment.

NOTE

If connector plate is left off 1J5, PRIMARY POWER DISCONNECT SWITCH 1S2 (Figure 3-2) will have to be jumpered or held depressed in order for primary power to be supplied to the terminal.

8. Adjust INPUT LOOP ADJUST Control A5R2 to supply the desired current, as indicated on the voltohmmeter.

9. Refer to Figure 3-1. Place METER FUNCTION SELECTOR W1S1 in LOOP IN position.

10. Refer to Figure 5-4 (Sheet 3 of 3). Adjust INPUT LOOP METER CAL. ADJ. Control X4R1 until current indicated on front panel FUNCTION DISPLAY METER 1M1 is identical to that of the voltohmmeter.

11. Disconnect voltohmmeter from 1J5-3 and -7 and their mating spade lugs. Reconnect spade lug to 1J5-3 and -7.

12. Remove jumper connected 1J5-2 and -5.

13. Replace cover on 1J5 and reset terminal controls for normal operation.

c. Input Loop and Loop In Meter Adjustment (TTY Mode).

CAUTION

The connections described in subsequent steps a.1 through a. should be accomplished prior to applying power to any of the equipment described.

1. Connect the terminal for TTY operation.

NOTE

The terminal input and output must not be connected in Common Loop Mode. Also, if a TTY is not in the loop, complete the loop by substituting a 100 ohm, 2 watt resistor in its place.

2. Refer to Figure 3-2. Remove cover from INPUT/OUTPUT TERMINAl CONNECTOR 1J5.

3. Unscrew and disconnect terminal spade lug connection to 1J5-3 (DATA IN connection). Connect the positive lead of a voltohmmeter (Simpson Model 260, or equivalent) to the disconnected terminal spade lug.

4. Connect the common voltohmmeter lead to the 1J5-3 terminal connection.

5. Set the voltohmmeter to the 100 MA range.

6. Rotate INPUT LOOP ADJUST CONTROL A5R2 completely ccw.

7. Apply power to the equipment.

NOTE

If a connector plate is left off of 1J5, PRIMARY POWER DISCONNECT SWITCH 1S2 (Figure 3-2) will have to be jumpered or held depressed in order for primary power to be supplied to the terminal.

8. Adjust INPUT LOOP ADJUST Control A5R2 to supply the desired current, as indicated on the voltohmmeter.

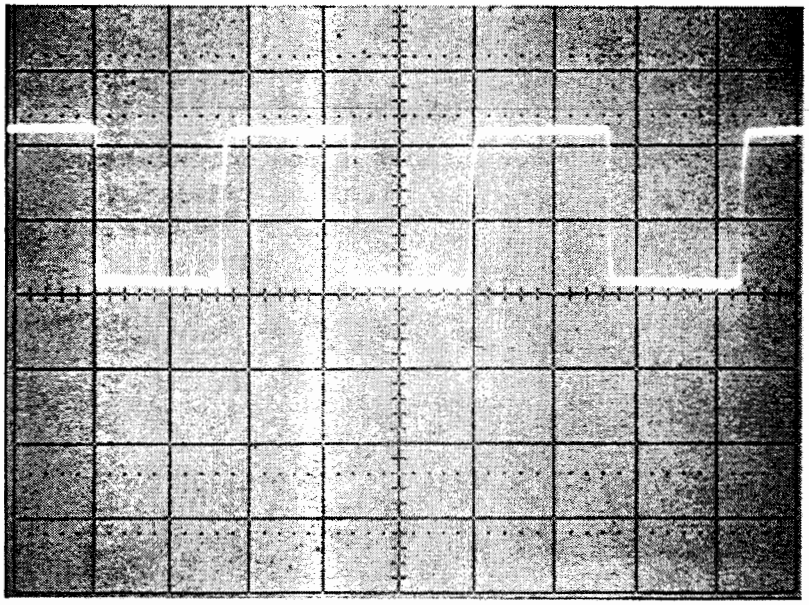
9. Refer to Figure 3-1. Place METER FUNCTION SELECTOR W1S1 in LOOP IN position.

10. Refer to Figure 5-4 (Sheet 3 of 3). Adjust INPUT LOOP METER CAL. ADJ. Control X4R1 until current indicated on front panel FUNCTION DISPLAY METER 1M1 is identical to that of the voltohmmeter.

11. Disconnect voltohmmeter from 1J5-3 and its mating spade lug. Reconnect spade lug to 1J5-3.

12. Replace cover on 1J5 and reset terminal control for normal operation.

Table 5-1. A1TP1 - MODULATOR 200X MARK TONE TEST POINT TYPICAL DATA



Data Measured

10 To 11 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 300 kHz

200X MARK TONE Test Point A1TP1

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1 : 2000 Hz
TONE SELECTION (Hz) - SHIFT FREQUENCY Switches A7S1 : ±500 Hz
Transmit Controls (Keyline and Sense) : Not Significant
Receive Controls : Not Significant

B. Data Input: Not Significant

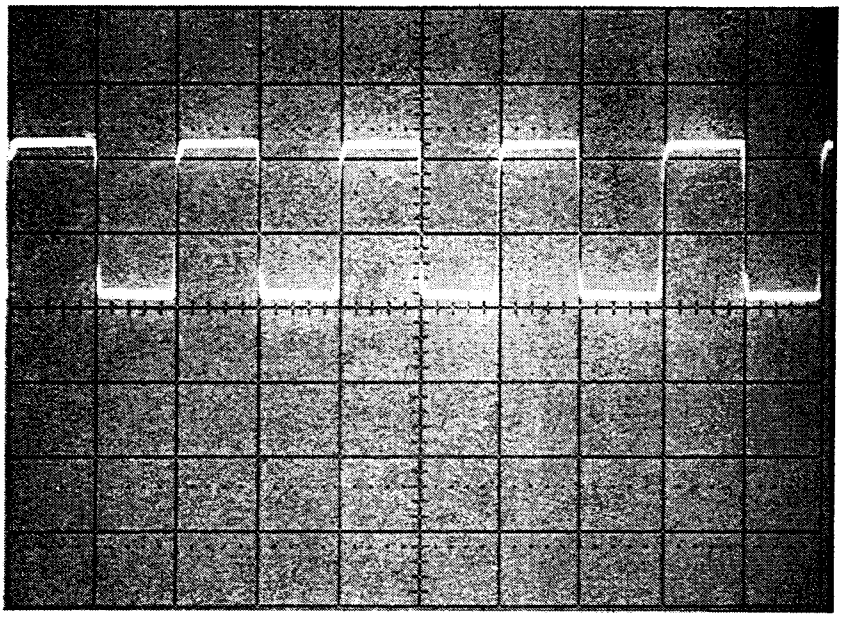
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 1 μ sec/centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All Measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to Odbm.
3. Internal triggering may be used unless otherwise specified.

Table 5-2. A1TP2 - MODULATOR 200X SPACE TONE TEST POINT TYPICAL DATA



Data Measured

20 to 11 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 500 kHz

200X SPACE TONE Test Point A1TP2

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1 : 2000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
Transmit Controls (Keyline and Sense): Not Significant
Receive Controls: Not Significant

B. Data Input: Not Significant

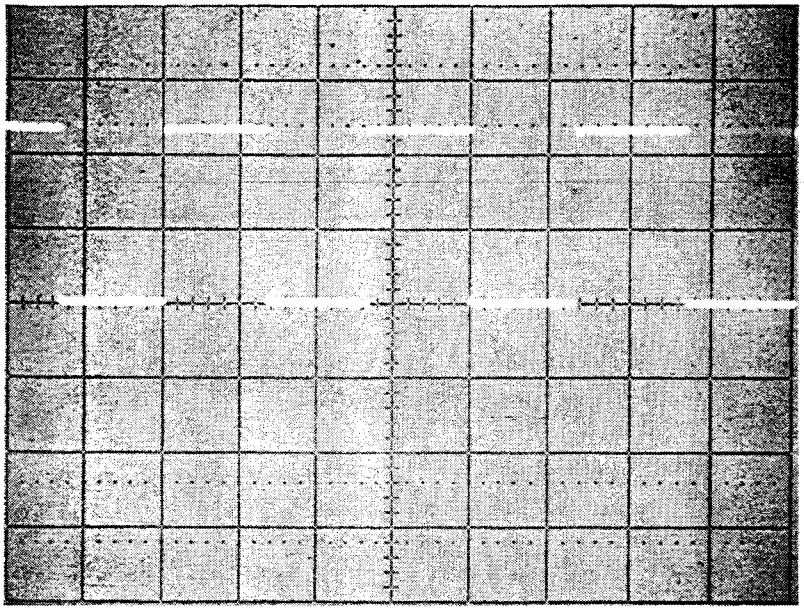
C. Oscilloscope Control Positions

Vertical: 5 Volts/ Centimeter, dc coupled
Horizontal: Sweep Speed = 1 μ sec/centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-3. A1TP3 - MODULATOR TX DATA TEST POINT TYPICAL DATA



Data Measured
10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 37.5 Hz

TX DATA Test Point A1TP3

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: Not Significant
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: Not Significant
Transmit Controls (Keyline and Sense): Not Significant
Receive Controls: Not Significant

B. Data Input

1 : 1 Mark/Space data was applied at the RS-232
Input or TTY Data Input; 75 Baud

C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 10 milliseconds/centimeter

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-4. A1TP4 - MODULATOR CMOS SEND TEST POINT TYPICAL DATA

The data measured at A1TP4 is a CMOS Logic Level Low when an RS-232 Logic Level Low is applied to rear panel Input/Output Connection W3J3-4. This data becomes a CMOS Logic Level High when an RS-232 Logic Level High is applied to W3J3-4.

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: Not Significant
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: Not Significant
Transmit Controls (Keyline and Sense): Not Significant
Receive Controls: Not Significant

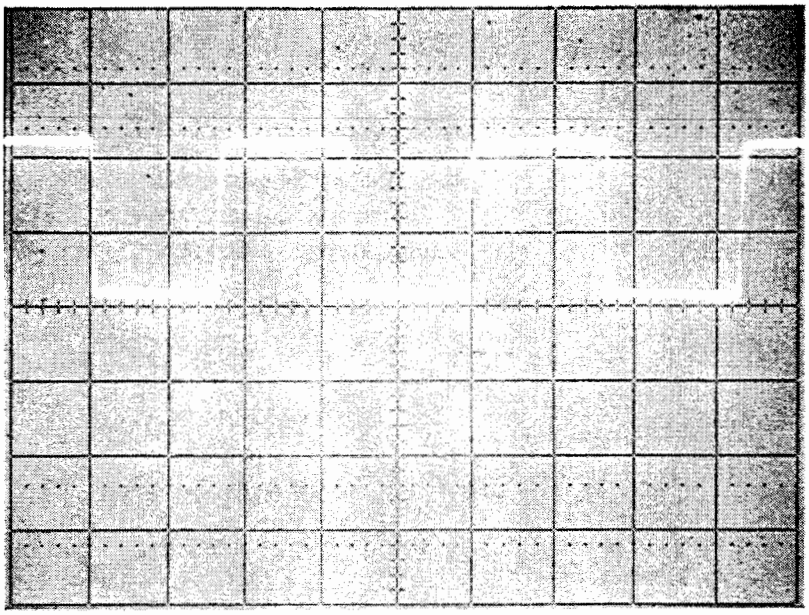
B. Data Input: Not Significant

C. Oscilloscope Control Positions: Not Significant

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-5. A1TP5 - MODULATOR 200X AUDIO OUTPUT TEST POINT TYPICAL DATA - MEASUREMENT NO. 1



Data Measured

10 to 11 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 300 kHz

200X AUDIO OUTPUT Test Point A1TP5 - Measurement No. 1

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: Not Significant
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: Not Significant
TRANSMIT-KEYLINE CLOSED/OPEN/AUTO Switch A6S1: Not Significant
TRANSMIT-SENSE NORM/REV/OFF Switch A6S2: OFF or NORM
Receive Controls: Not Significant

B. Data Input: Not Significant

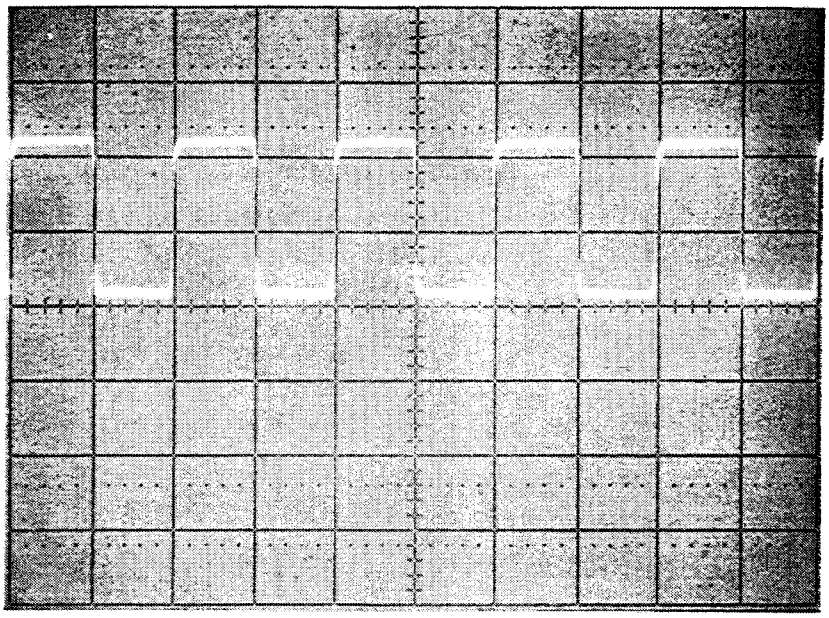
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 1 μ sec/centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-6. A1TP5 - MODULATOR 200X AUDIO OUTPUT TEST POINT TYPICAL DATA - MEASUREMENT NO. 2



Data Measured

10 to 11 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 500 kHz

200X audio output Test Point A1TP5 - Measurement No. 2

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: Not Significant
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: Not Significant
TRANSMIT-KEYLINE CLOSED/OPEN/AUTO Switch A6S1: OPEN
TRANSMIT-SENSE NORM/REV/OFF Switch A6S2: REV
Receive Controls: Not Significant

B. Data Input: Not Significant

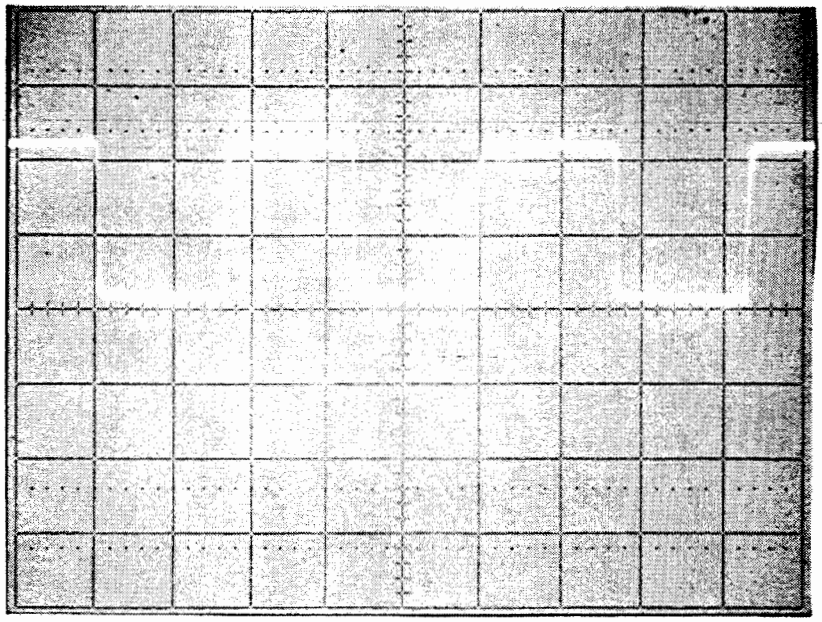
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: Sweet Speed = 1 μ sec/centimeter
Horizontal: Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-7. A1TP5 - MODULATOR 200X AUDIO OUTPUT TEST POINT TYPICAL DATA - MEASUREMENT NO. 3



Data Measured
10 to 11 Volts, Peak-to-Peak
0 Volts = Center Scale
Frequency = 300 kHz

200X AUDIO OUTPUT Test Point A1TP5 - Measurement No. 3

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: Not Significant
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: Not Significant
TRANSMIT-KEYLINE CLOSED/OPEN/AUTO Switch A6S1: OFF
TRANSMIT-SENSE NORM/REV/OFF Switch A6S2: OFF or NORM
Receive Controls: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

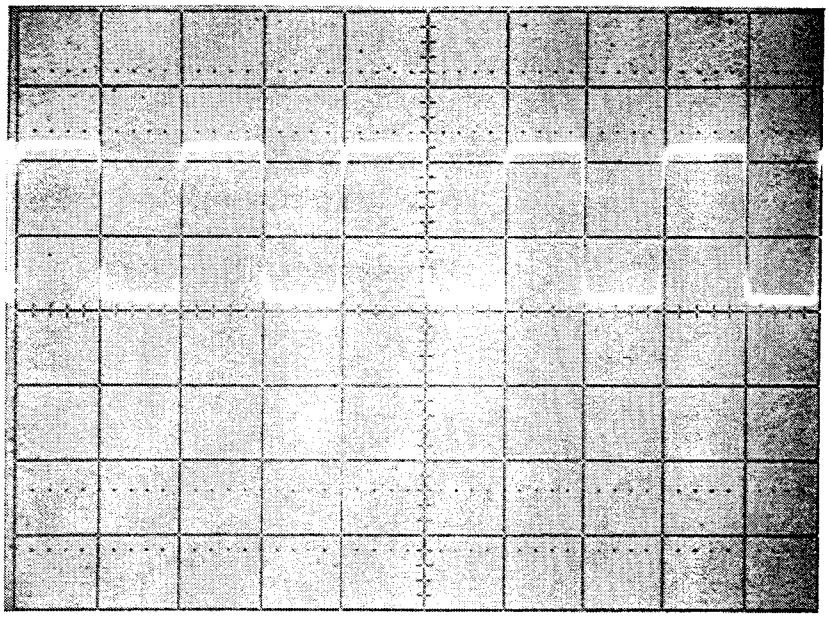
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 1 μ sec/centimeter
Trigger = Normal Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-8. A1TP5 - MODULATOR 200X AUDIO OUTPUT TEST POINT TYPICAL DATA - MEASUREMENT NO. 4



Data Measured

10 to ll Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 500 kHz

200X AUDIO OUTPUT Test Point A1TP5 - Measurement No. 4

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: Not Significant
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: Not Significant
TRANSMIT-KEYLINE CLOSED/OPEN/AUTO Switch A6S1: OFF
TRANSMIT-SENSE NORM/REV/OFF Switch A6S2: REV
Receive Controls: Not Significant

B. Data Input: 1 : 1 Mark/Spcea, 75 Baud

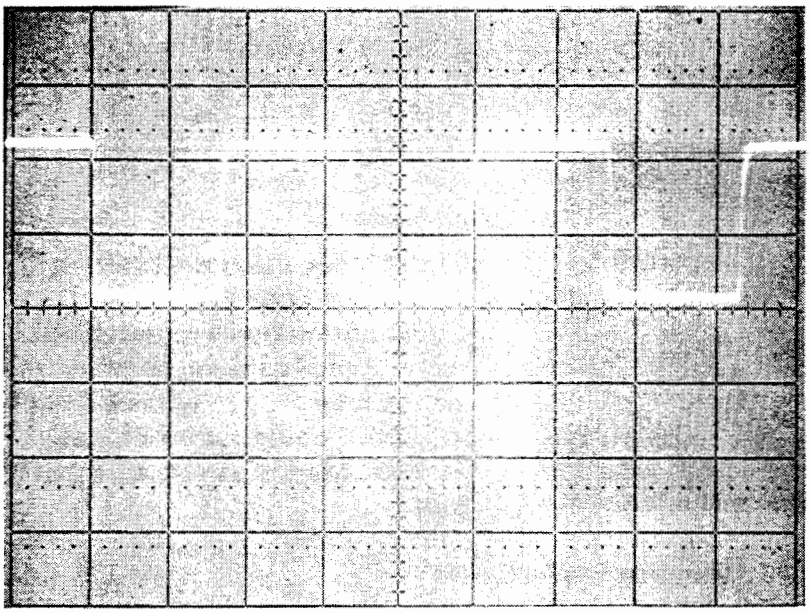
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 1 μ sec/centimeter
Trigger = Normal Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-9. A1TP5 - MODULATOR 100X AUDIO OUTPUT TEST POINT TYPICAL DATA - MEASUREMENT NO. 5



Data Measured

10 to 11 Volts, Peak-to-Peak
0 Volts = Center Scale
Frequency = 300 kHz

200X AUDIO OUTPUT Test Point A1TPS - Measurement No. 5

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: Not Significant
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: Not Significant
TRANSMIT - KEYLINE CLOSED/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
Receive Controls: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

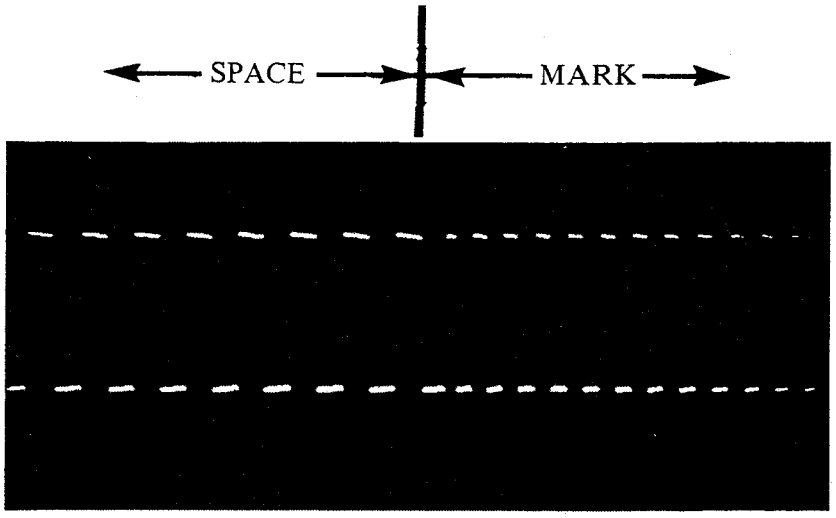
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 1 μ sec/centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-10. A1TP5 - MODULATOR 200X AUDIO OUTPUT TEST POINT TYPICAL DATA - MEASUREMENT NO. 6



Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale
The transition between the Space and the Mark tone is shown in the center of the scale (that is, Space Tone is shown on the left half, Mark Tone on the right half).

200X AUDIO OUTPUT Test Point A1TP5 - Measurement No. 6

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCIY Switches A7S1: Not Significant
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: Not Significant
TRANSMIT - KEYLINE CLOSED/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
Receive Controls: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

C. Oscilloscope Control Positions

Delayed Sweep
External Trigger using data transitions as the trigger
Main Sweep Speed: 2 milliseconds/centimeter
Delayed Sweep Speed: 5 μ seconds/centimeter

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.

Table 5-11. A1TP6 - MODULATOR STEP SINUSOID TEST POINT TYPICAL DATA - MEASUREMENT NO. 1

No Tone Is Present at STEP SINUSOID
Test Point A1TP6

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 1000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
IDLE SELECT Switch A1S1: "M" Position (Mark Hold)
TRANSMIT - KEYLINE CLOSED/OPEN/AUTO Switch A6S1: Not Significant
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: OFF
Receive Controls: Not Significant

B. Data Input: Inactive (Mark Hold Condition exists)

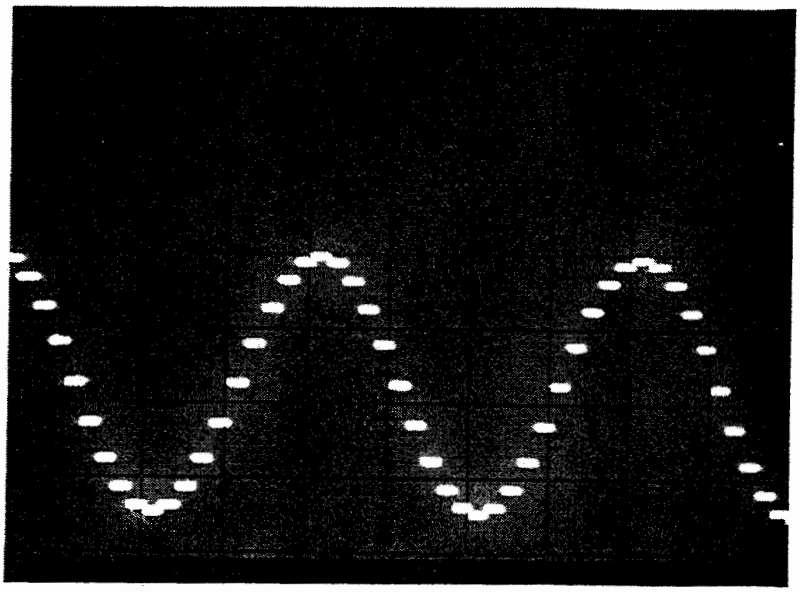
C. Oscilloscope Control Positions

Vertical: 1 Volt/Centimeter
Horizontal: Sweep Speed = 0.5 Milliseconds/Centimeter

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-12. A1TP6 - MODULATOR STEP SINUSOID TEST POINT TYPICAL DATA - MEASUREMENT NO. 2



Data Measured

Frequency = 500 Hz

STEP SINUSOID Test Point A1TP6 - Measurement No. 2

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 1000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
IDLE SELECT Switch A1S1: "M" Position (Mark Hold)
TRANSMIT - KEYLINE CLOSED/OPEN/AUTO Switch A6S1: Not Significant
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
Receive Controls: Not Significant

B. Data Input: Inactive (Mark Hold Condition exists)

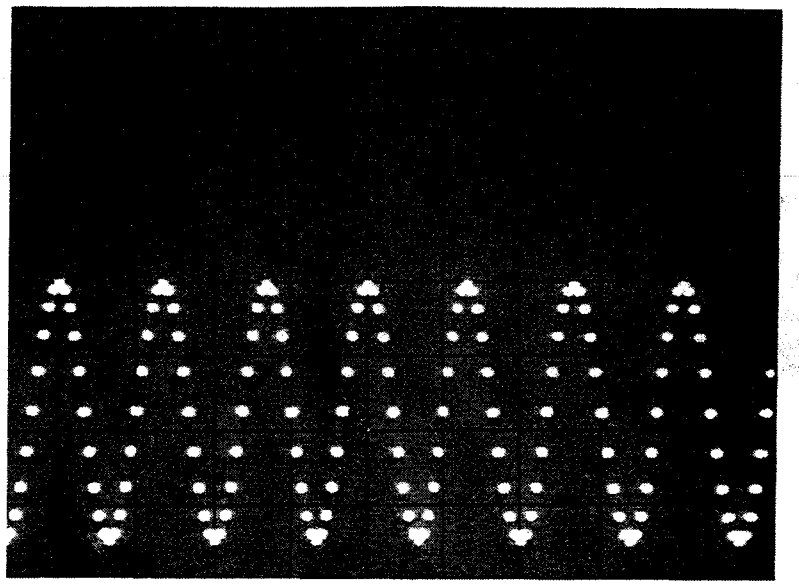
C. Oscilloscope Control Positions:

Vertical: 1 Volt/Centimeter
Horizontal: Sweep Speed = 0.5 Milliseconds/Centimeter

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

Table 5-13. A1TP6 - MODULATOR STEP SINUSOID TEST POINT TYPICAL DATA - MEASUREMENT NO. 3



Data Measured

Frequency = 1500 Hz

STEP SINUSOID Test Point A1TP6 - Measurement No. 3

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 1000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
IDLE SELECT Switch A1S1: "M" Position (Mark Hold)
TRANSMIT - KEYLINE CLOSED/OPEN/AUTO Switch A6S1: Not Significant
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: REV
Receive Controls: Not Significant

B. Data Input: Inactive (Mark Hold Condition exists)

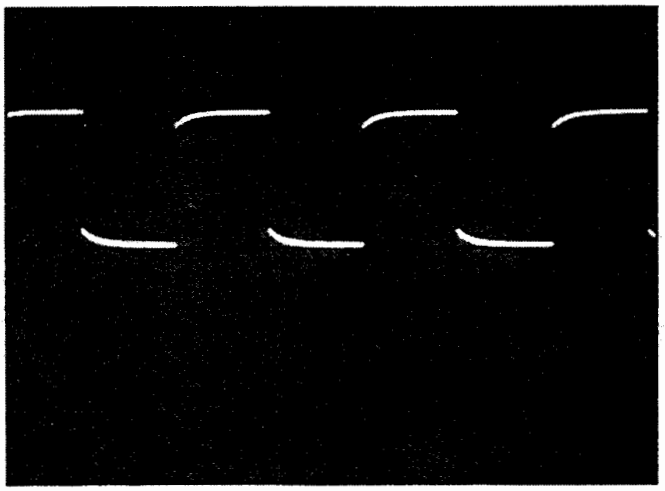
C. Oscilloscope Control Positions

Vertical: 1 Volt/Centimeter
Horizontal: Sweep Speed = 0.5 Milliseconds/Centimeter

D. Notes

1. All Measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Modulator output was adjusted to 0dBm.
3. Internal triggering may be used unless otherwise specified.

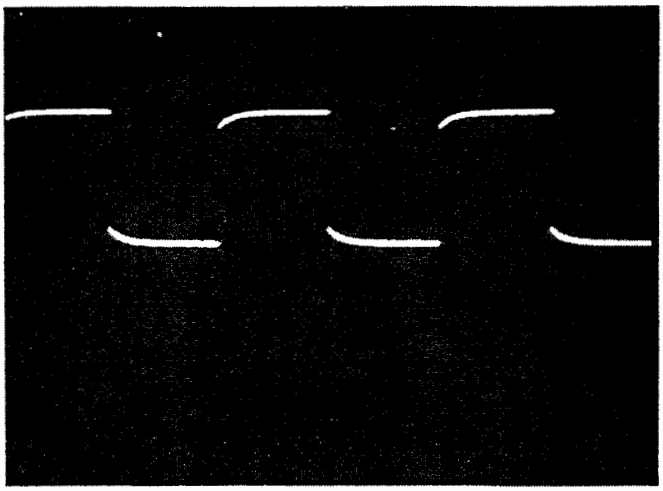
Table 5-14. A2TP1 AND A2TP2 - DEMODULATOR MARK L.O. FREQ. AND SPACE L.O. FREQ. TEST POINTS (RESPECTIVELY) TYPICAL DATA



MARK L.O. FREQ. Test Point A2TP1

Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 6500 Hz



SPACE L.O. Test Point A2TP2

Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 5500 Hz

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 2000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
Transmit Controls: Not Significant
Receive Controls: Not Significant

B. Data Input: Not Significant

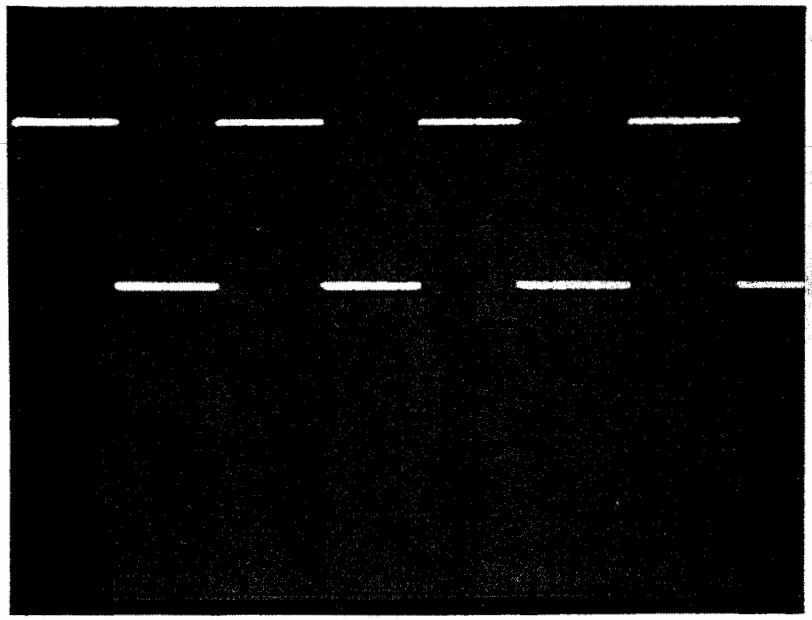
C. Oscilloscope Control Positions

Vertical: 5 Volts Centimeter, dc coupled
Horizontal: 50 Microseconds Centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Internal triggering may be used unless otherwise specified.

Table 5-15. A2TP3 - DEMODULATOR SLICER OUTPUT TEST POINT TYPICAL DATA



Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 37.5 Hz

SLICER OUTPUT Test Point A2TP3

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 0000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch S6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HELD/REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 10 Milliseconds/Centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Internal triggering may be used unless otherwise specified.

Table 5-16. A2TP4 - DEMODULATOR VALID DATA DET. TEST POINT TYPICAL DATA

The data at VALID DATA DET. Test Point A2TP4 is a CMOS Level High when data is received, and a CMOS Level Low when data is no longer received or when invalid data is detected.

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 2000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM or REV
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: Not Significant

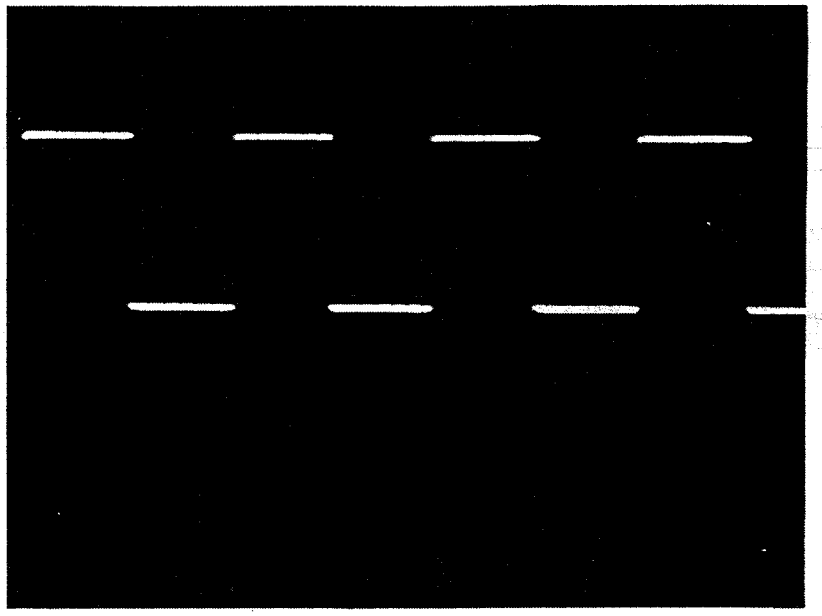
B. Data Input: 1 : 1 Mark/Space, 75 Baud

C. Oscilloscope Control Positions: Not Significant

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Internal triggering may be used unless otherwise specified.

Table 5-17. A2TP5 - DEMODULATOR CMOS RCV DATA TEST POINT TYPICAL DATA



Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 37.5 Hz

NOTE

When RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3 is set to Mark Hold position, this data becomes a CMOS Logic Level CMOS REV DATA Test Point A2TP5 Low.

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 2000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM or REV
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: NORM or REV

B. Data Input: 1 : 1 Mark/Space, 75 Baud

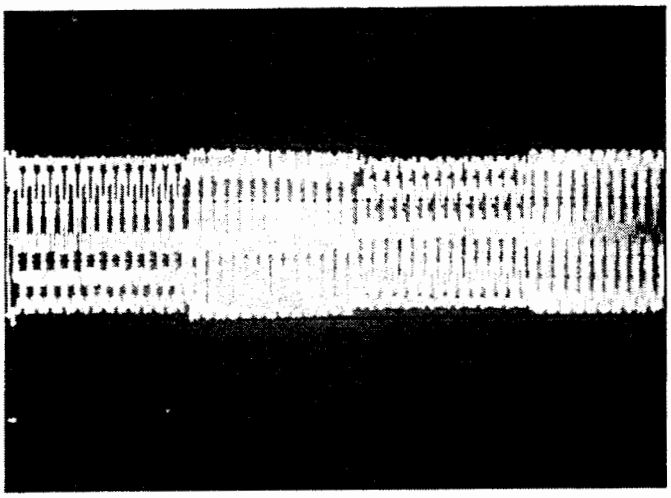
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 10 Milliseconds/Centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Internal triggering may be used unless otherwise specified.

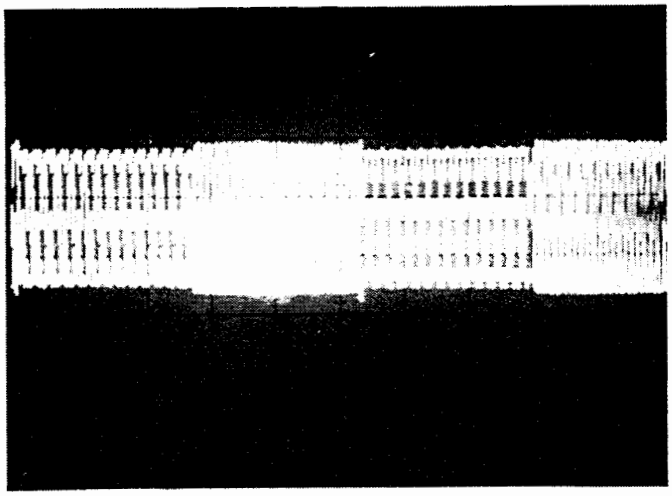
Table 5-18. A2TP6 AND A2TP7 - DEMODULATOR MARK MIX. OUT AND SPACE MIX. OUT TEST POINTS (RESPECTIVELY) TYPICAL DATA



MARK MIX. OUT Test Point A2TP6

Data Measured

Approximately 1.4 Volts Peak-to-Peak
0 Volts = Center Scale



SPACE MIX. OUT Test Point A2TP7

Data Measured

Approximately 1.4 Volts Peak-to-Peak
0 Volts = Center Scale

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 2000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

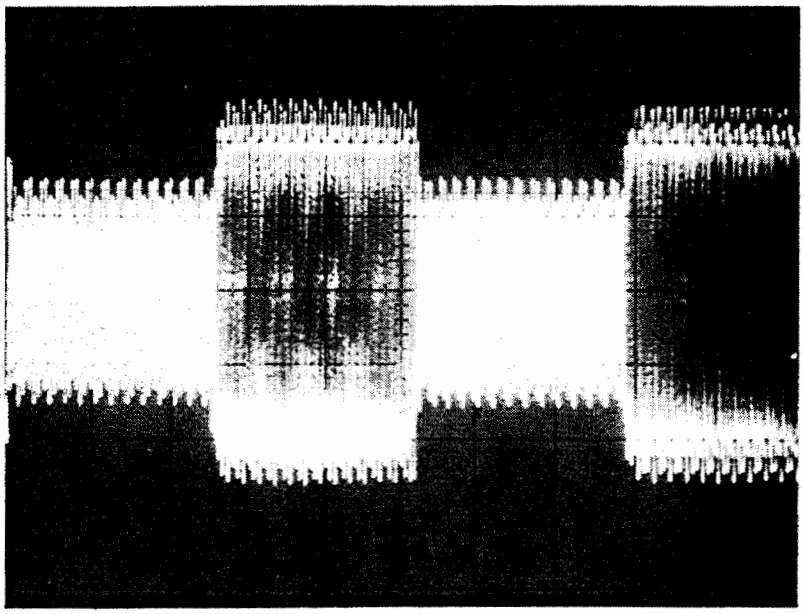
C. Oscilloscope Control Positions

Vertical: .5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 5 Milliseconds/Centimeter
Trigger = External, using positive data transitions as the trigger

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

Table 5-19. A2TP8 - DEMODULATOR SAA TEST POINT TYPICAL DATA



Data Measured

0 Volts = Center Scale

SAA Test Point A2TP8

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 2000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

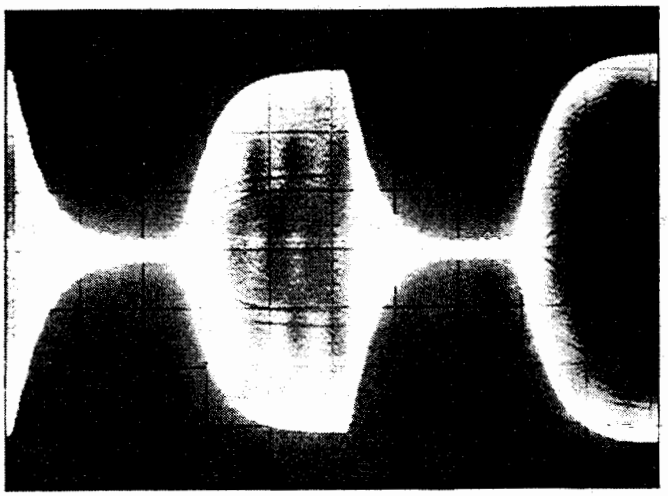
C. Oscilloscope Control Positions

Vertical: .5 Volts/Centimeter, ac coupled
Horizontal: Sweep Speed = 5 Milliseconds/Centimeter
Trigger = External, using data transitions as the trigger

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

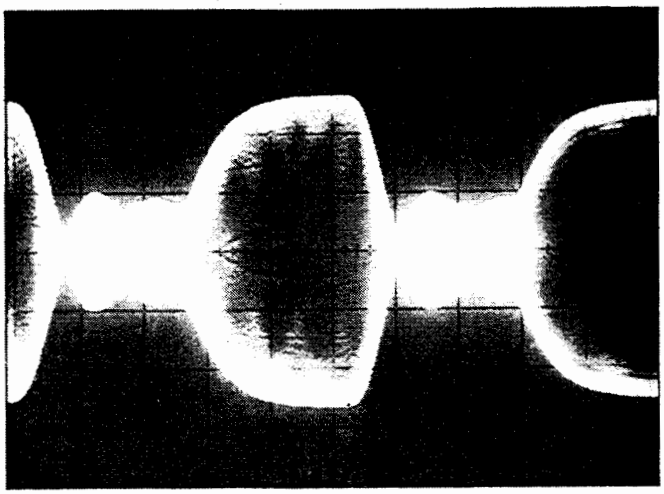
Table 5-20. A2TP9 - DEMODULATOR SPACE BPF OUT TEST POINT TYPICAL DATA



SPACE BPF OUT Test Point A2TP9
(C_f = 2000 Hz, S_f = ± 500 Hz)

Data Measured

3 Volts Peak-to-Peak
0 Volts = Center Scale



SPACE BPF OUT Test Point A2TP9
(C_f = 2000 Hz, S_f = ± 100 Hz)

Data Measured

2.6 Volts Peak-to-Peak
0 Volts = Center Scale

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: As indicated
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: As indicated
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

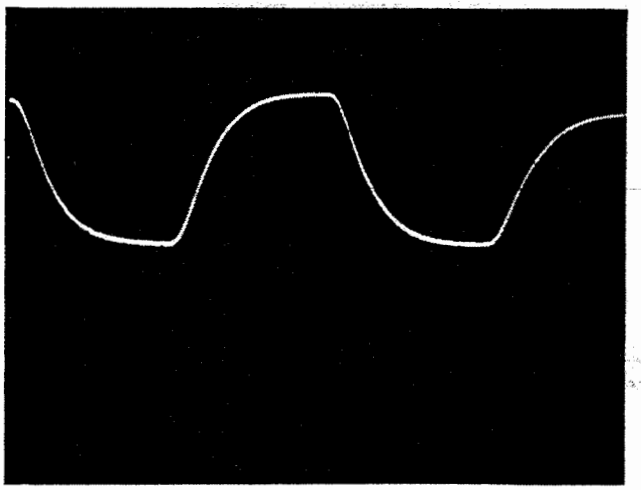
C. Oscilloscope Control Positions

Vertical: .5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 5 Milliseconds/Centimeter
Trigger = External, using data transitions as the trigger

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

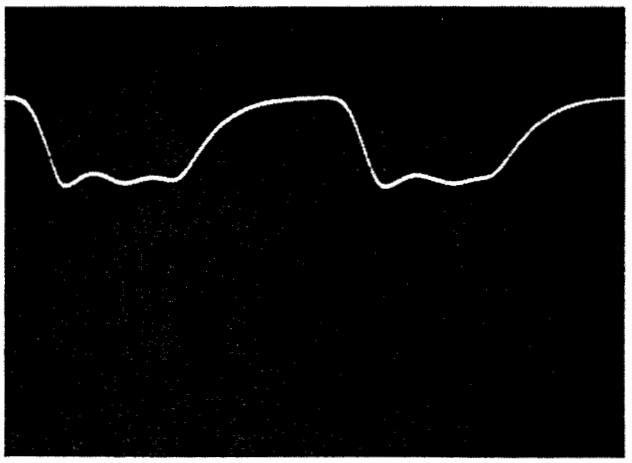
TABLE 5-21. A2TP10 - DEMODULATOR SPACE ENVELOPE TEST POINT TYPICAL DATA



SPACE ENVELOPE TEST Point A2TP10
(C_f = 2000 Hz, S_f = 500 Hz)

Data Measured

5.2 Volts Peak-to-Peak
0 Volts = Center Scale



SPACE ENVELOPE Test Point A1TP10
(C_f = 2000 Hz, S_f = ± 100 Hz)

Data Measured

3.2 Volts Peak-to-Peak
0 Volts = Center Scale

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: As indicated
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: As indicated
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

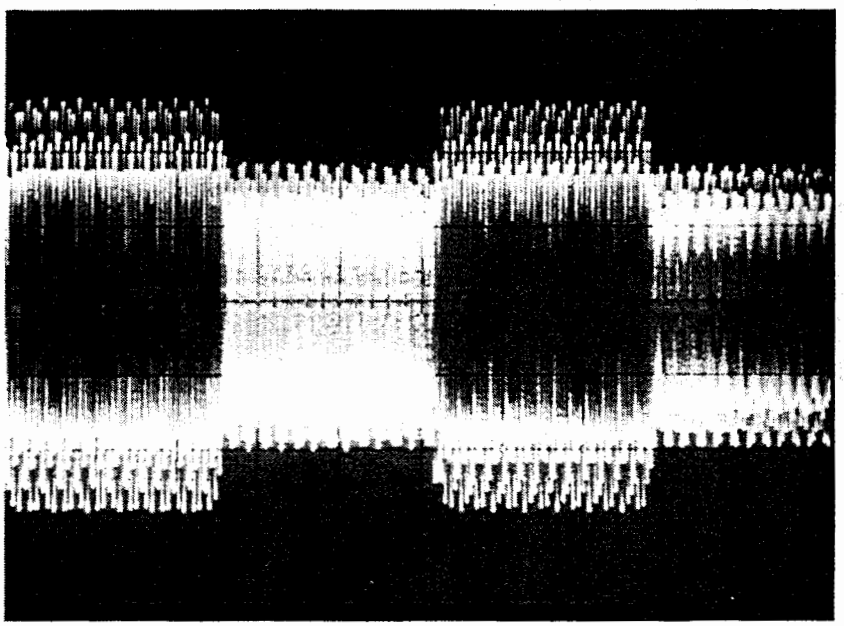
C. Oscilloscope Control Positions

Vertical: 2 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 5 Milliseconds/½centimeter
Trigger = External, using data transitions as the trigger

D. Notes

1. All measurements have been made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

Table 5-22. A2TP11 - DEMODULATOR MAA TEST POINT TYPICAL DATA



Data Measured

0 Volts = Center Scale

MAA Test Point A2TP11

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches, A7S1: 2000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S11: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

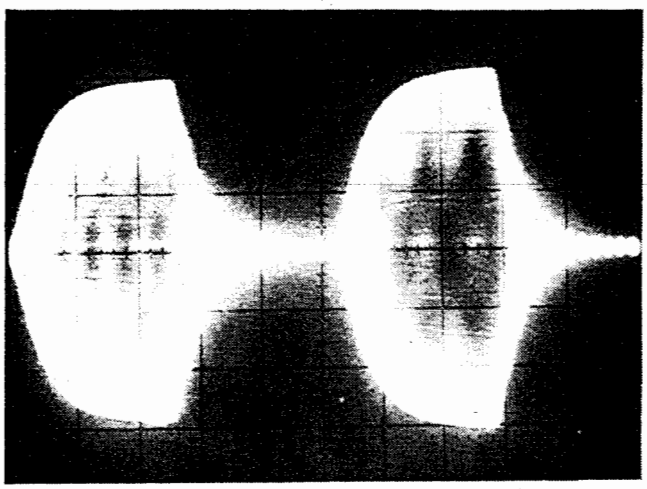
C. Oscilloscope Control Positions

Vertical: .5 Volts/Centimeter, ac coupled
Horizontal: Sweep Speed = 5 Milliseconds/Centimeter
Trigger = External, using data transitions as the trigger

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

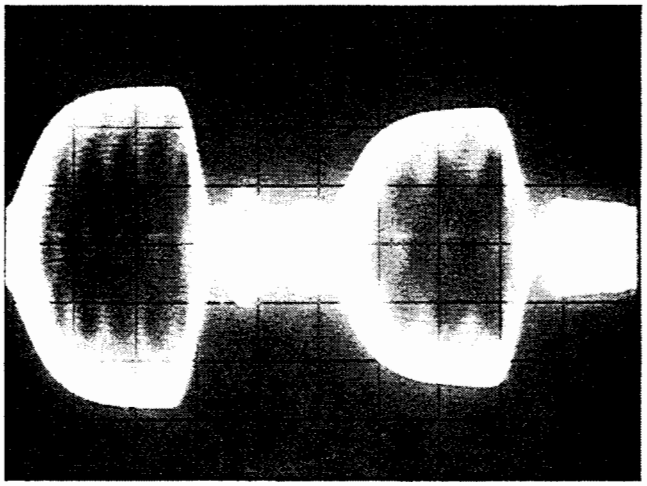
Table 5-23. A2TP12 - DEMODULATOR MARK BPF OUT TEST POINT TYPICAL DATA



MARK BPF OUT Test Point A2TP12
(C_f = 2000 Hz, S_f = ± 500 Hz)

Data Measured

3 Volts Peak-to-Peak
0 Volts = Center Scale



MARK BPF OUT Test Point A2TP12
(C_f = 2000 Hz S_f = ± 100 Hz)

Data Measured

2.6 Volts Peak-to-Peak
0 Volts = Center Scale

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: As indicated
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: As indicated
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

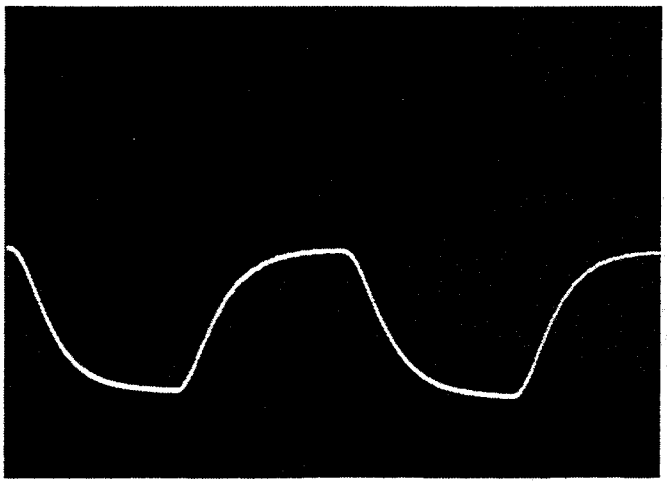
C. Oscilloscope Control Positions

Vertical: .5 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 5 Milliseconds/Centimeter
Trigger = External, using data transitions as the trigger

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

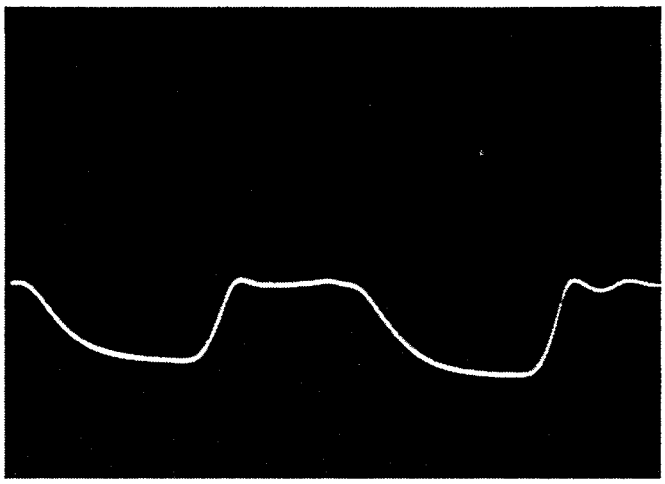
TABLE 5-24. A2TP13 - DEMODULATOR MARK ENVELOPE TEST POINT TYPICAL DATA



MARK ENVELOPE Test Point A2TP13
(C_f = 2000 Hz, S_f = ± 500 Hz)

Data Measured

5.2 Volts Peak-to-Peak
0 Volts = Center Scale



MARK ENVELOPE Test Point A2TP13
(C_f = 2000 Hz, S_f = ± 100 Hz)

Data Measured

3.6 Volts Peak-to-Peak
0 Volts = Center Scale

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: As indicated
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: As indicated
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

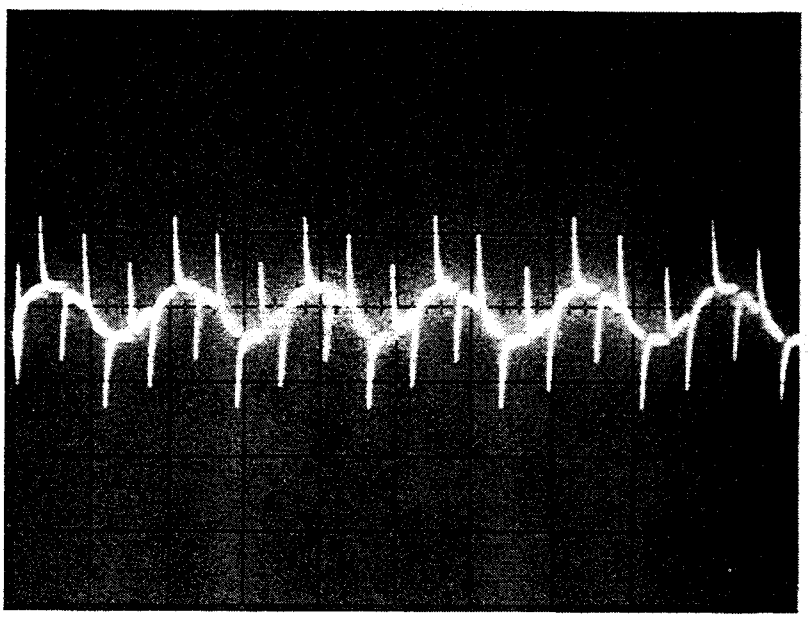
C. Oscilloscope Control Positions

Vertical: 2 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 5 Milliseconds/Centimeter
Trigger - External, using data transitions as the trigger

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

Table 5-25. A2TP14 - DEMODULATOR DECISION LEVEL TEST POINT TYPICAL DATA



Data Measured

0 Volts = Center Scale

DECISION LEVEL Test Point A2TP14

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: 2000 Hz
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: ± 500 Hz
TRANSMIT - KEYLINE CLOSE/OPEN/AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HOLD/REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

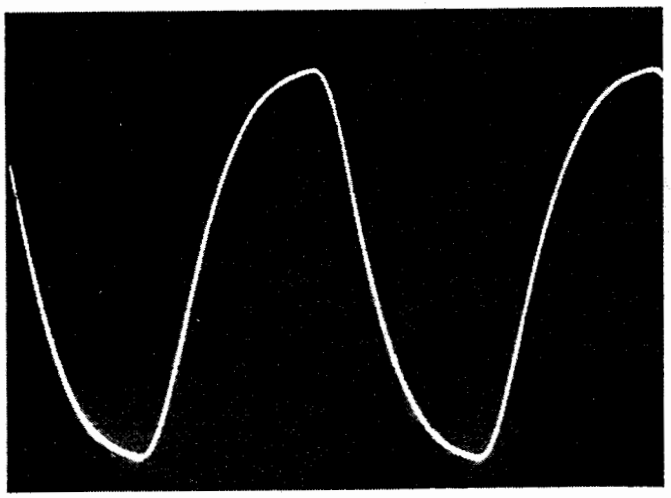
C. Oscilloscope Control Positions

Vertical: .2 Volts/Centimeter, dc coupled
Horizontal: Sweep Speed = 50 Milliseconds/Centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Internal triggering may be used unless otherwise specified.

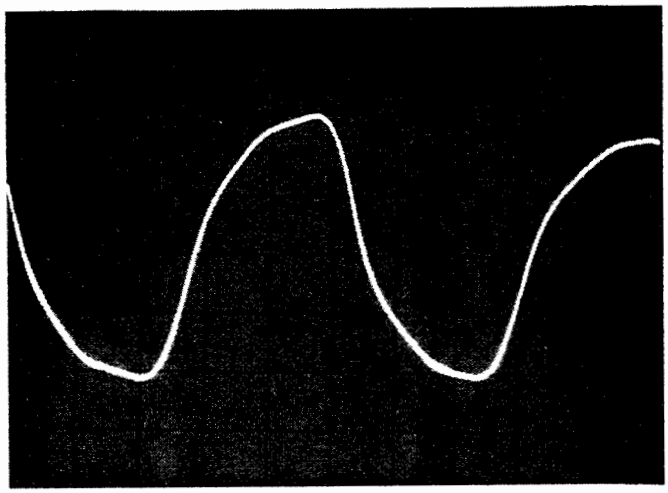
Table 5-26. A2TP15 and A2TP16 - Demodulator COMPOSITE ENVELOPE and GAIN CONT. V Test Points (respectively) Typical Data



COMPOSITE ENVELOPE Test Point A2TP15
(C_f = 2000 Hz, S_f = ± 500 Hz)

Data Measured

6.8 Volts Peak-to-Peak
0 Volts = Center Scale



COMPOSITE ENVELOPE Test Point A1TP15
(C_f = 2000 Hz, S_f = ± 100 Hz)

Data Measured

4.4 Volts Peak-to-Peak
0 Volts = Center Scale

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: As indicated
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: As indicated
TRANSMIT - KEYLINE CLOSE OPEN AUTO Switch A6S1: AUTO or CLOSED
TRANSMIT - SENSE NORM/REV/OFF Switch A6S2: NORM
RECEIVE - SENSE NORM/MARK HOLD REV Switch A6S3: Not Significant

B. Data Input: 1 : 1 Mark/Space, 75 Baud

C. Oscilloscope Control Positions

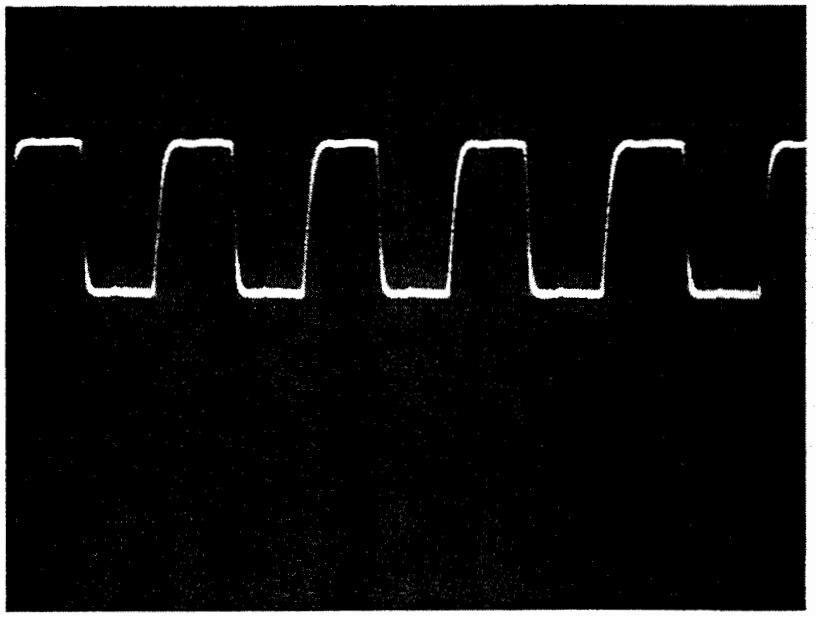
Vertical: 1 Volt/Centimeter, dc coupled
Horizontal: Sweep Speed = 50 Milliseconds/Centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Internal triggering may be used unless otherwise specified.

Measured Data - GAIN CONT V, Test Point A2TP16: This test point will indicate a negative dc level. This level controls the conduction of AGC FET A2Q3.

Table 5-27. A3TP1 - TIMING AND CONTROL OSC. OUT TEST POINT TYPICAL DATA



Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 1.024 MHz

OSC. OUT Test Point A3TP1

A. Terminal Control Position

Transmit Controls: Not Significant
Receive Controls: Not Significant
Tone Selection: Not Significant

B. Data Input: Not Significant

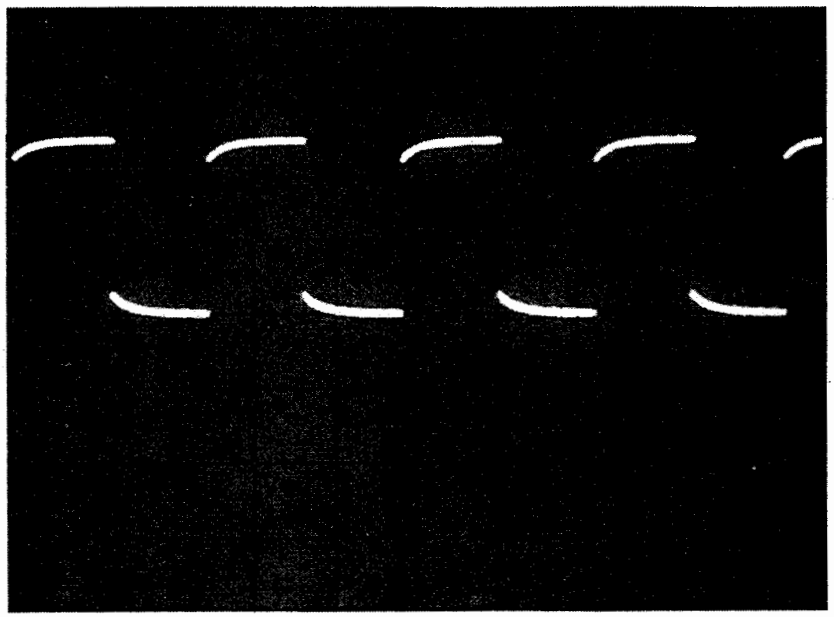
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: .5 Microseconds/Centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Internal triggering may be used unless otherwise specified.

Table 5-28. A3TP2 - TIMING AND CONTROL 8 KHZ TEST POINT TYPICAL DATA



Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale
Frequency = 8 KHz

8 KHZ Test Point A3TP2

A. Terminal Control Positions

Transmit Controls: Not Significant
Receive Controls: Not Significant
Tone Selection: Not Significant

B. Data Input: Not Significant

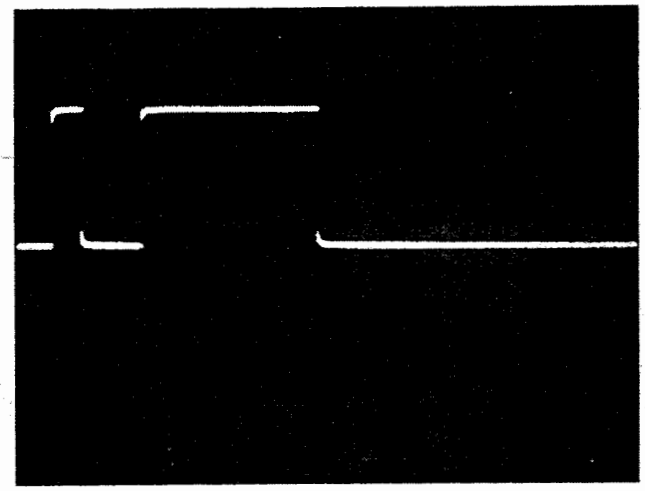
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: 50 Microseconds/Centimeter
Trigger = Normal, Positive Edge

D. Notes

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.
2. Internal triggering may be used unless otherwise specified.

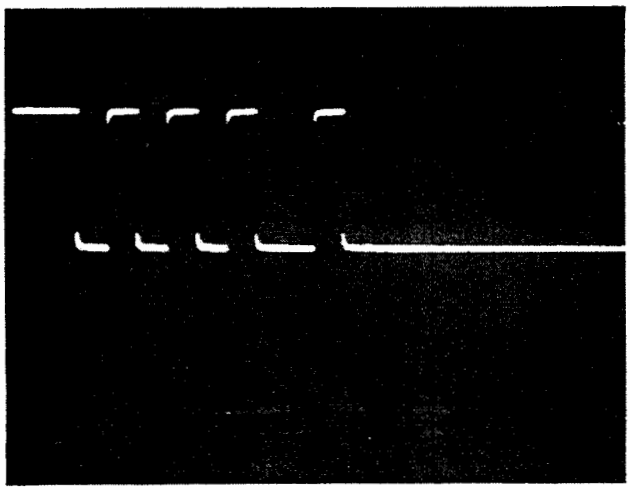
Table 5-29. A3TP3 - TIMING AND CONTROL C + S TEST POINT TYPICAL DATA



C + S Test Point A3TP3
(C_f = 1965 Hz, S_f = ± 560 Hz)

Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale



C + S Test Point A3TP3
(C_f = 2690 Hz, S_f = ± 2975 Hz)

Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: As indicated
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: As indicated
Transmit Controls: Not Significant
Receive Controls: Not Significant

B. Data Input: Not Significant

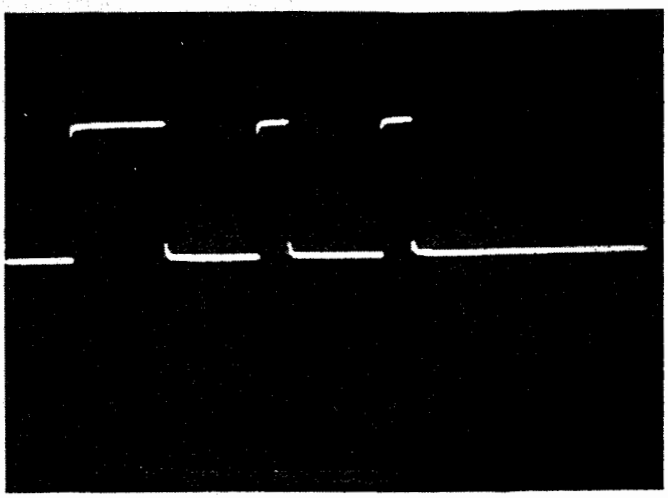
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: .5 Milliseconds Centimeter
Trigger = External, trigger on negative edge of A3U16-4

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

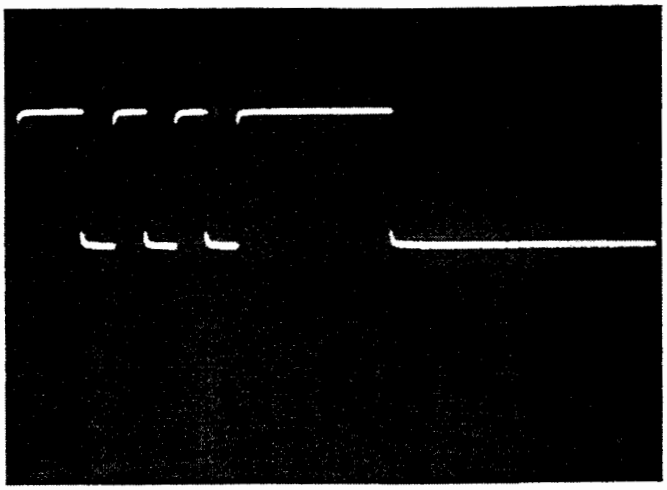
Table 5-30. A3TP4 - TIMING AND CONTROL I - (C + S) TEST POINT TYPICAL DATA



I - (C + S) Test Point A3TP4
(C_f = 1965 Hz, S_f = ± 560 Hz)

Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale



I - (C + S) Test Point A3TP4
(C_f = 2690 Hz, S_f = ± 2975 Hz)

Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: As indicated
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: As indicated
Transmit Controls: Not Significant
Receive Controls: Not Significant

B. Data Input: Not Significant

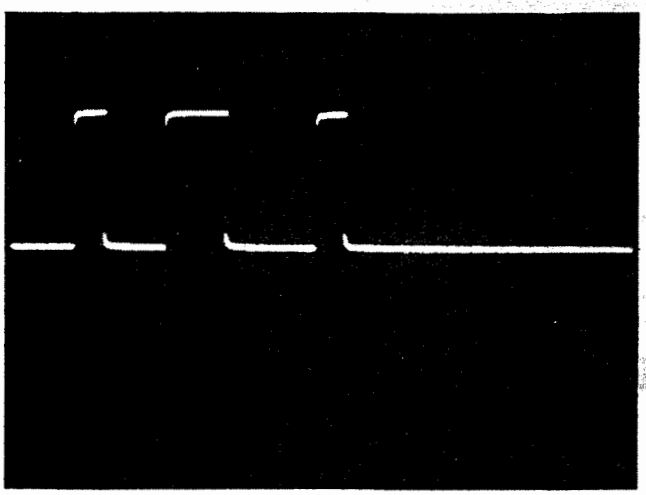
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: .5 Milliseconds/Centimeter
Trigger = External, trigger on negative edge of A3U16-4.

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

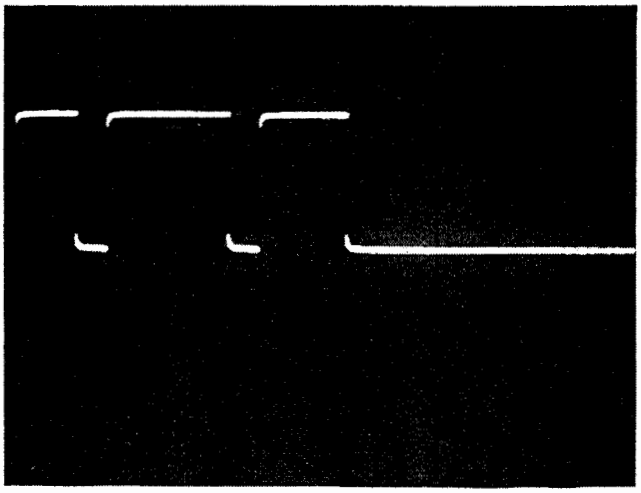
Table 5-31. A3TP5 - TIMING ANC CONTROL C - S TEST POINT TYPICAL DATA



Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale

C - S Test Point A3TP5
(C_f = 1965 Hz, S_f = ± 560 Hz)



Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale

C - S Test Point A3TP5
(C_f = 2690 Hz, S_f = ± 2975 H)

A. Terminal Control Positions

TONE SELECTION (Hz) - CENTER FREQUENCY Switches A7S1: As indicated
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: As indicated
Transmit Controls: Not Significant
Receive Controls: Not Significant

B. Data Input: Not Significant

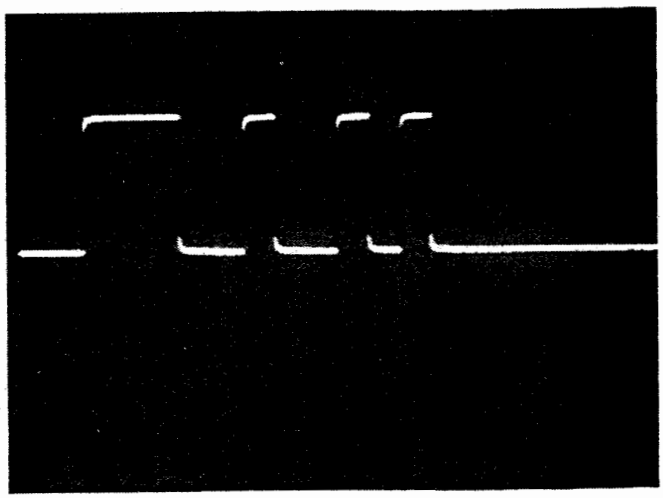
C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: .5 Milliseconds/Centimeter
Trigger = External, trigger on negative edge of A3U16-4.

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

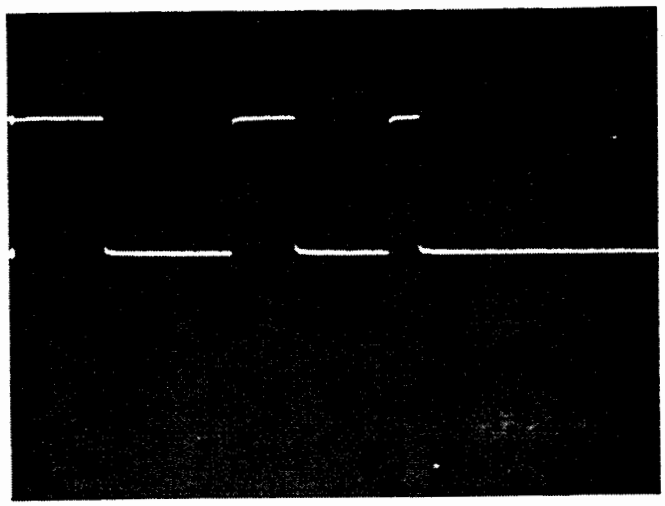
Table 5-32. A3TP6 - TIMING AND CONTROL I - (C-S) TEST POINT TYPICAL DATA



I - (C-S) Test Point A3TP6
(C_f = 1965 Hz, S_f = ± 560 Hz)

Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale



I - (C-S) Test Point A3TP6
(C_f = 2690 Hz, S_f = ± 2975 Hz

Data Measured

10 to 12 Volts Peak-to-Peak
0 Volts = Center Scale

A. Terminal Control Positions

TONE SELECTION (Hz) - Center frequency Switches A7S1: As indicated
TONE SELECTION (Hz) - SHIFT Frequency Switches A7S1: As indicated
Transmit Controls: Not Significant
Receive Controls: Not Significant

B. Data Input: Not Significant

C. Oscilloscope Control Positions

Vertical: 5 Volts/Centimeter, dc coupled
Horizontal: .5 Milliseconds/Centimeter
Trigger = External, trigger on negative edge of A3U16-4

D. Note

1. All measurements were made with LOOPBACK/NORM Switch 1S3/A5S1 in LOOPBACK position.

SECTION 6

PARTS LISTS AND COMPONENT LOCATION DRAWINGS

6.1 INTRODUCTION

This section contains the parts lists and component location drawings for the RF-3352 FSK Terminal. (Schematic drawings are contained in Section 7 of this manual.)

6.2 MANUFACTURERS' CODE-TO-ADDRESS DATA

The sourse of each component is given in five digit form in the parts lists. Manufacturers' Code 14304 applies to the Harris Corporation, RF Communications Division, 1700 University Avenue, Rochester, New York 14610. Manufacturers' Code 81349 applies to Military specifications (parts) promulgated by Military Departments/Agencies under authority of Defense Standardization Manual 4120 3-M.

Table 6-1. CHASSIS/PANEL ASSEMBLY PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
A1	Modulator PWB Assembly	14304	6918-1120
A2	Demodulator PWB Assembly	14304	6918-1130
A3	Timing and Control PWB Assembly	14304	6918-1140
A4	Interface PWB Assembly	14304	6918-1150
A5	Transistor/Regulator PWB Assembly	14304	6918-1190
A6	Control and Indicator PWB Assembly	14304	6918-1210
A7	Frequency Control Board Assembly	14304	6918-1220
1CB1	Switch, ON-OFF	14304	S90-0008-000
1J1	Connector, Power	81349	MS3102R-14S-02P
1J2	Connector, Auto-Start	81349	MS3102-10SL-3P
1J5	Connector, Interconnection	14304	J41-0003-010
1K1	Relay	14304	K10-0001-000
1M1	Meter	14304	6918-1202
PS1	Power Supply PWB Assembly	14304	6918-1160
1S1	Switch, 115/230 Volt Select	14304	S30-0005-000
1S2	Switch, Interlock	14304	S80-0003-000
1T1	Transformer	14304	6918-1118
W1	Interconnect PWB Assembly	14304	6918-1110
W2	Chassis and Panel Wiring Assembly	14304	6918-0110
W3	RS-232 Interface Wiring Assembly	14304	6918-0130
W4	Low Level Wiring Assembly	14304	6918-0140
1XK1	Socket, for Relay K1	14304	J30-0005-001

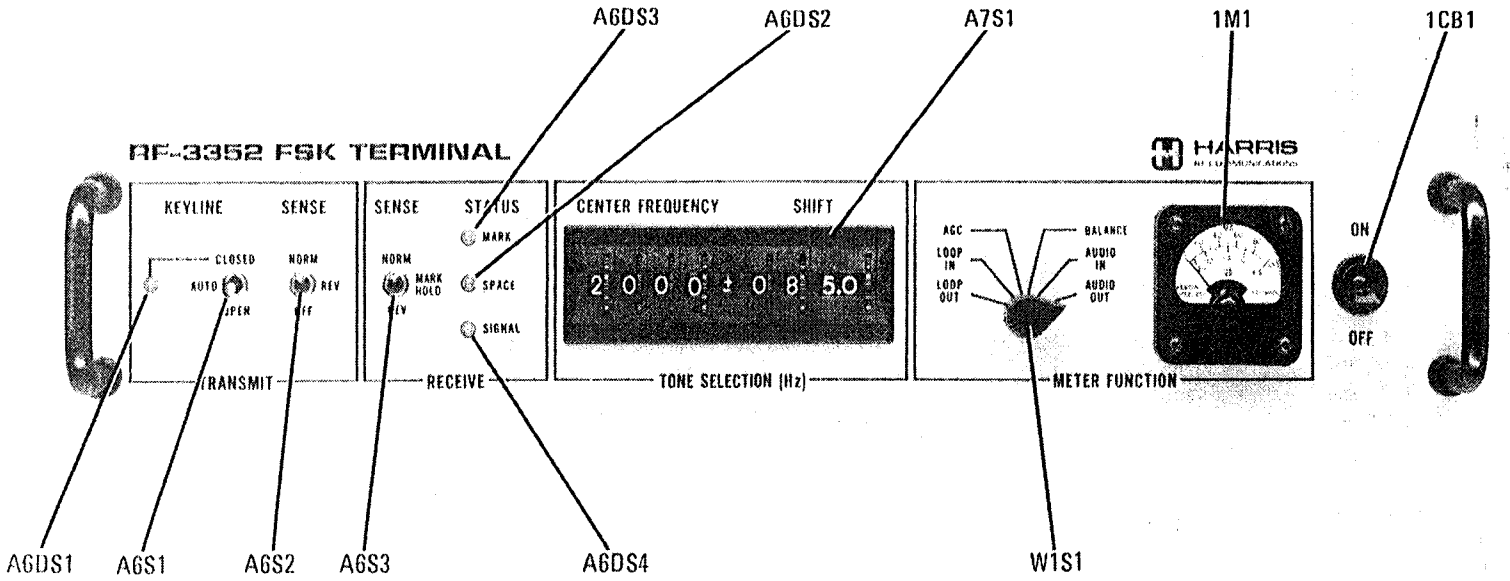


Figure 6-1. RF-3352 FSK Terminal Component Locations (Sheet 1 of 5)

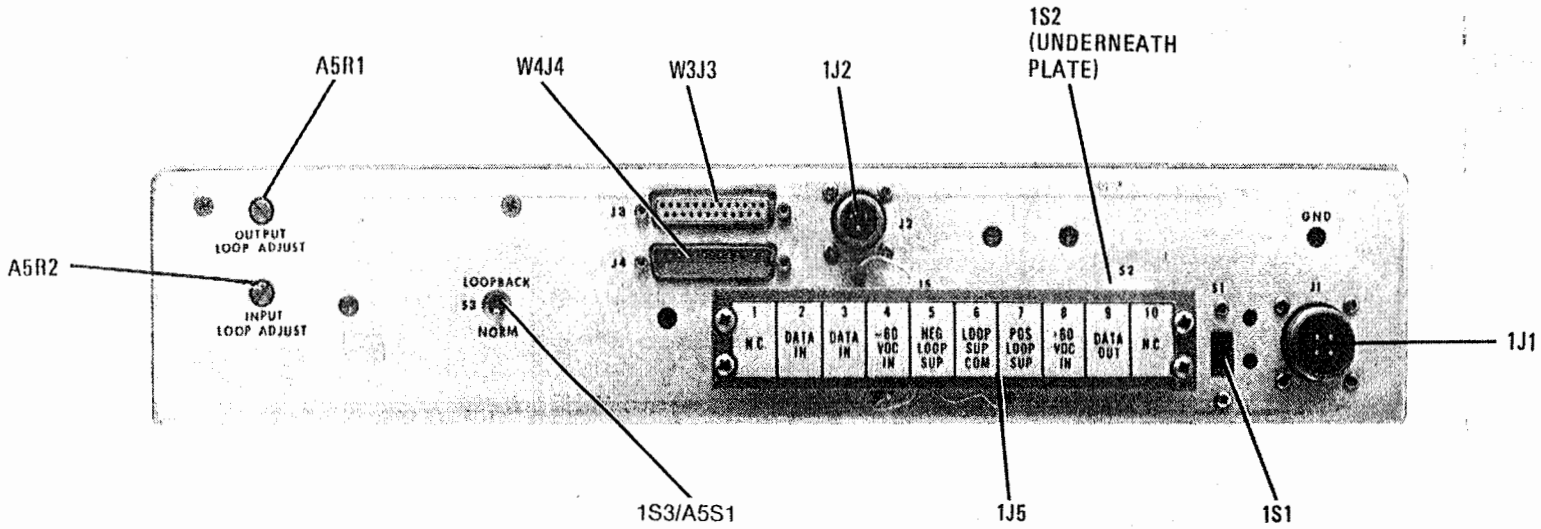


Figure 6-1. RF-3352 FSK Terminal Component Locations (Sheet 2 of 5)

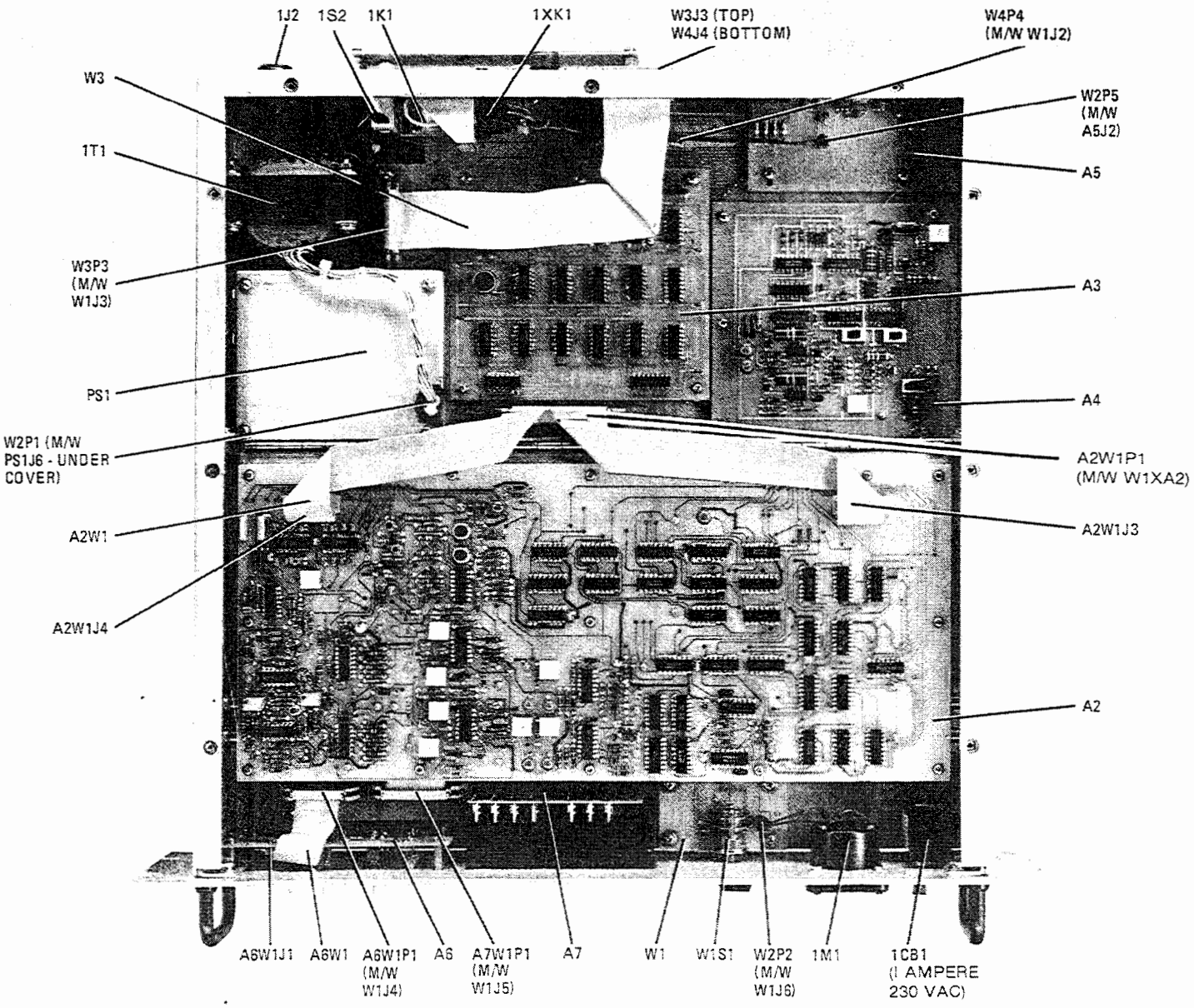


Figure 6-1. RF-3352 FSK Terminal Component Locations (Sheet 3 of 5)

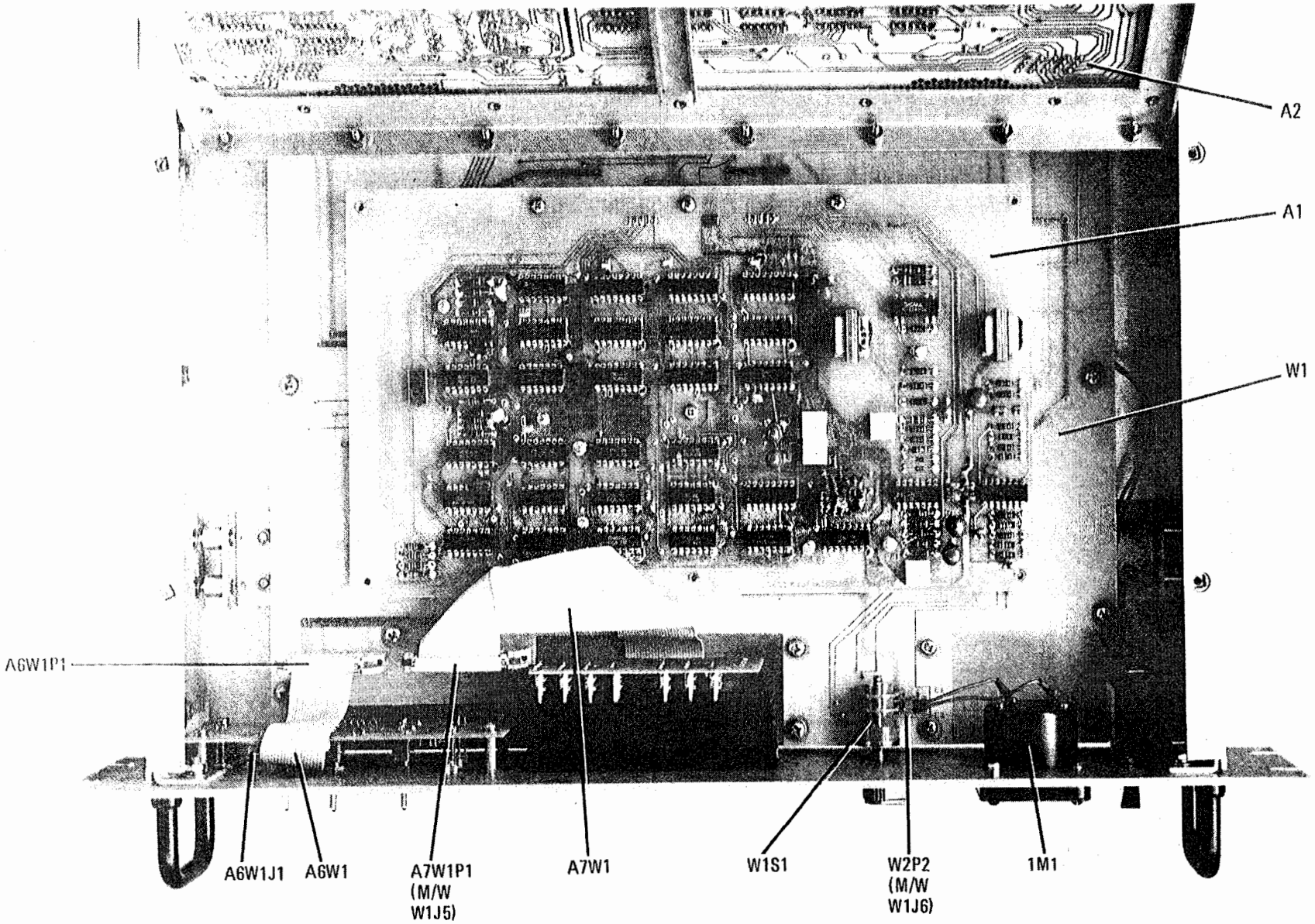


Figure 6-1. RF-3352 FSK Terminal Component Locations (Sheet 4 of 5)

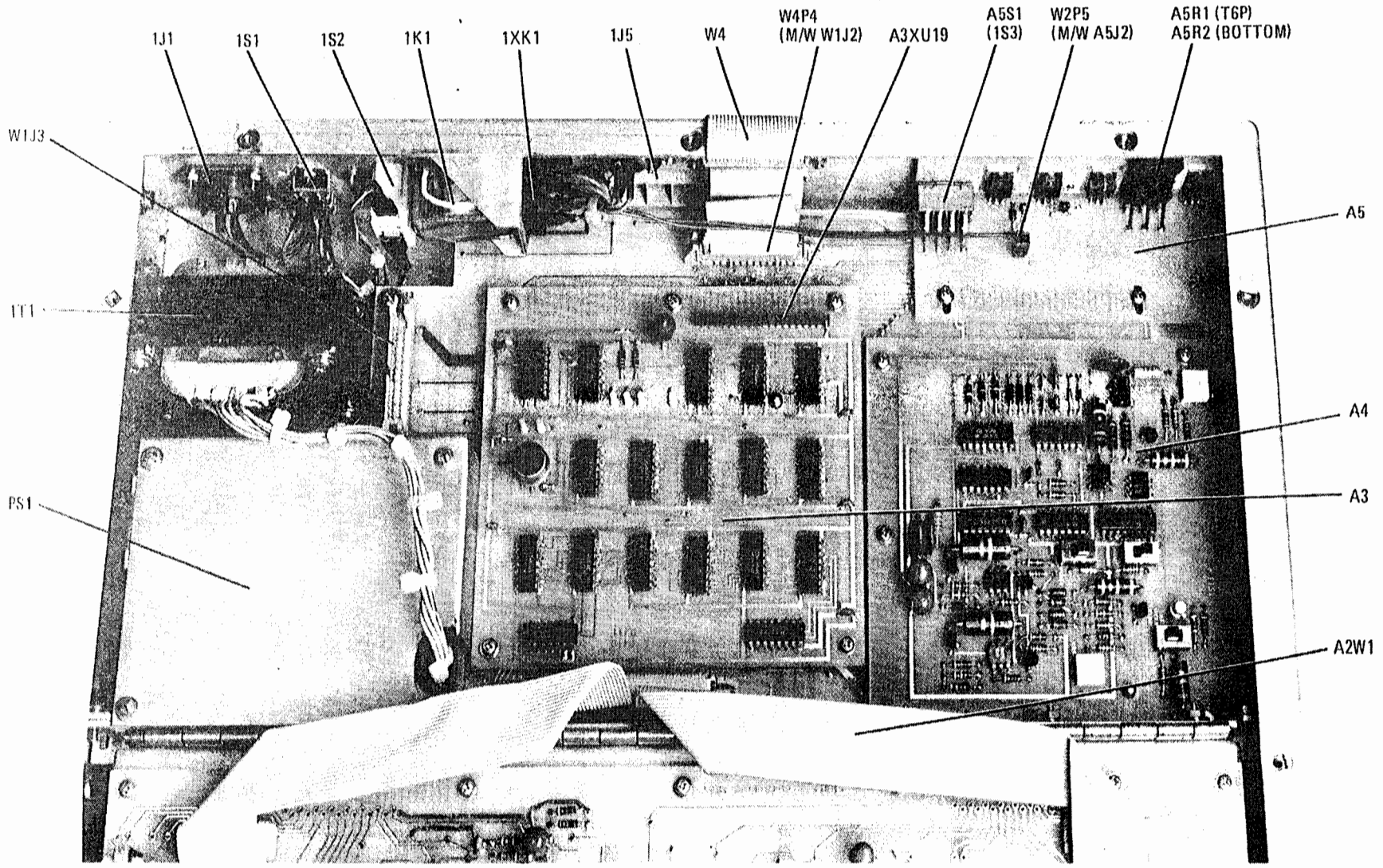
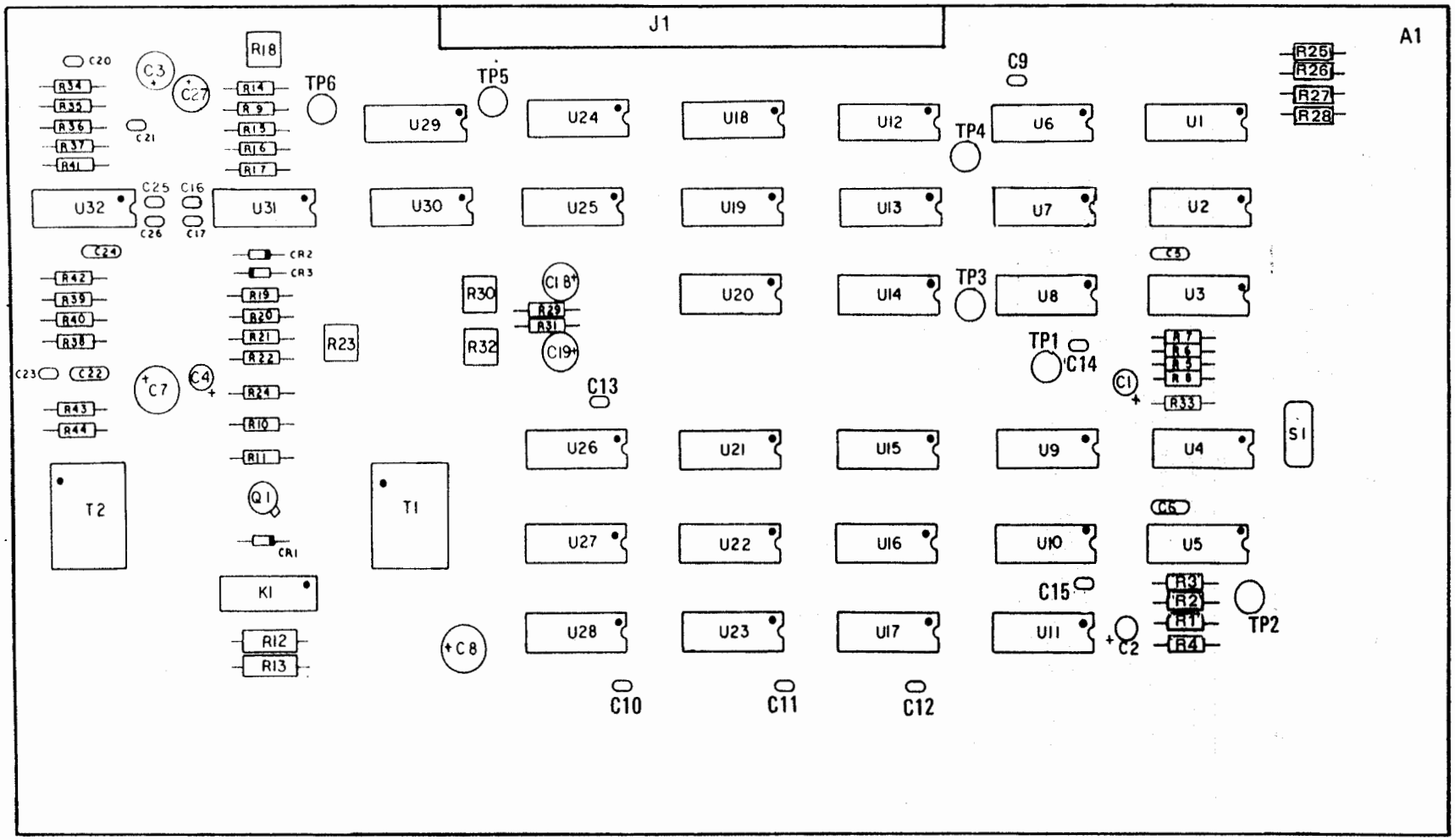


Figure 6-1. RF-3352 FSK Terminal Component Locations (Sheet 5 of 5)

Table 6-2. MODULATOR PWB A1 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
A1	Modulator PWB Assembly	14304	6918-1120
	(Note: Prefix all reference designators With A1)		
C1, C2	Capacitor, Tantalum, 3.3 uF, 10% 50 Vdcw	14304	C25-0002-010
C3	Capacitor, Tantalum, 22 uF, 10%, 50 Vdcw	14304	C25-0002-015
C4	Capacitor, Tantalum, 2.2 uF, 10%, 50 Vdcw	14304	C25-0002-009
C5, C6	Capacitor, Mica, 100 pF, 500 Vdcw	81349	CM04FD101J03
C7 C8	Capacitor, Tantalum, 22 uF, 10%, 50 Vdcw	14304	C25-0002-015
C9 to C15	Capacitor, Ceramic, .0l uF, 20%, 50 Vdcw	14304	C11-0005-103
C16, C17	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C18, C19	Capacitor, Tantalum, 15 uF, 10%, 50 Vdcw	14304	C25-0002-014
C20	Capacitor, Ceramic, .0033 uF, 5%, 100 Vdcw	14304	C11-0012-332
C21	Capacitor, Ceramic, .001 uF, 5%, 100 Vdcw	14304	C11-0012-102
C22	Capacitor, Ceramic, .022 uF, 5%, 100 Vdcw	14304	C11-0012-223
C23	Capacitor, Ceramic, .001 uF, 5%, 100 Vdcw	14304	C11-0012-102
C24	Capacitor, Ceramic, .01 uF, 5%, 100 Vdcw	14304	C11-0012-103
C25, C26	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C27	Capacitor, Tantalum, 22 uF, 10%, 50 Vdcw	14304	C25-0002-015
CR1	Diode, Rectifier, Type 1N4003	14304	D22-0001-000
CR2, CR3	Diode, Silicon, Type 1N4148	14304	D10-4148-000
K1	Relay, Reed Type, DPST	14304	K35-0001-000
Q1	Transistor, PNP Type	14304	Q02-2907-000
R1	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R2	Resistor, Fixed Composition, 560K ohms, 5%, 1/4W	81349	RCR07G564J
R3	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R4	Resistor, Fixed Composition, 1500 ohms, 5%, 1/4W	81349	RCR07G152J
R5	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R6	Resistor, Fixed Composition, 560K ohms, 5%, 1/4W	81349	RCR07G564J
R7	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R8	Resistor, Fixed Composition, 1500 ohms, 5%, 1/4W	81349	RCR07G152J
R9	Resistor, Fixed Composition, 680 ohms, 5%, 1/4W	81349	RCR07G681J
R10	Resistor, Fixed Composition, 2700 ohms, 5%, 1/4W	81349	RCR07G272J
R11	Resistor, Fixed Composition, 1000 ohms, 5%, 1/4W	81349	RCR07G102J
R12	Resistor, Fixed Composition, 430 ohms, 5%, 1/2W	81349	RCR20G431J
R13	Resistor, Fixed Composition, 270 ohms, 5%, 1/2W	81349	RCR20G271J
R14	Resistor, Fixed Composition, 100 ohms, 5%, 1/4W	81349	RCR07G101J
R15	Resistor, Fixed Composition, 16K ohms, 5%, 1/4W	81349	RCR07G163J
R16	Resistor, Fixed Composition, 11K ohms, 5%, 1/4W	81349	RCR07G113J
R17	Resistor, Fixed Composition, 16K ohms, 5%, 1/4W	81349	RCR07G163J



NOTE: FOR COMPONENT IDENTIFICATION, PREFIX ALL REFERENCE DESIGNATIONS WITH A1.

Figure 6-2. Modulator Pwb A1 Component Locations

Table 6-2. MODULATOR PWB A1 PARTS LIST (Cont.)

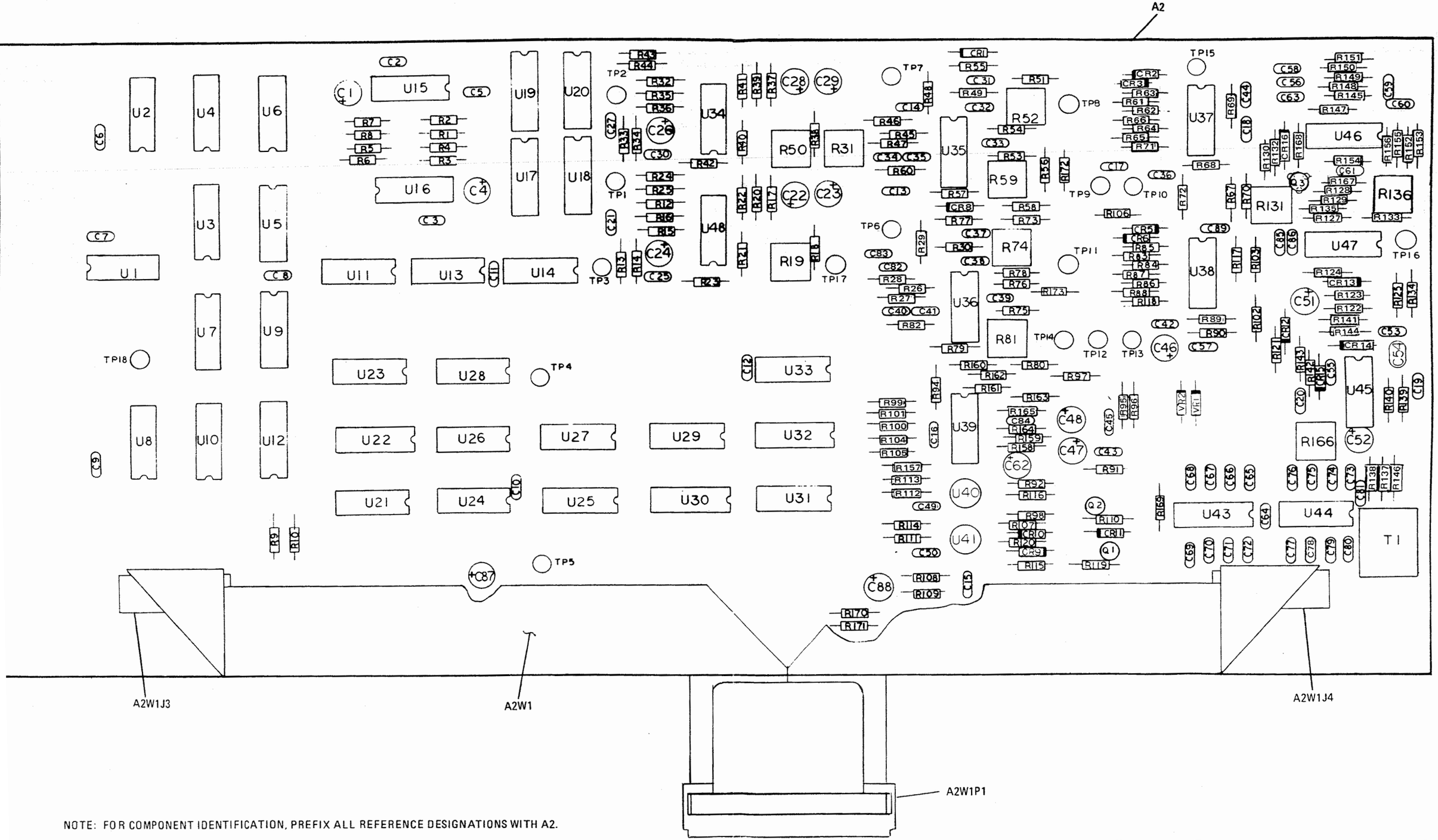
Ref. Desig.	Name and Description	Mfr.	Part No.
R18	Resistor, Variable 5K ohms	14304	R40-0008-502
R19	Resistor, Fixed Composition, 18K ohms, 5%, 1/4W	81349	RCR07G183J
R20, R21	Resistor, Fixed Composition, 1200 ohms, 5%, 1/4W	81349	RCR07G122J
R22	Resistor, Fixed Composition, 47K ohms, 5%, 1/4W	81349	RCR07G473J
R23	Resistor, Variable, 5K ohms	14304	R40-0008-502
R24	Resistor, Fixed Composition, 1000 ohms, 5%, 1/4W	81349	RCR07G102J
R25 -R28	Resistor, Fixed Composition, 33K ohms, 5%, 1/4W		RCR07G333J
R29	Resistor, Fixed Composition, 62K ohms, 5%, 1/4W	81349	RCR07G623J
R30	Resistor, Variable, 500K ohms	14304	R40-0008-504
R31	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R32	Resistor, Variable, 500K ohms	14304	R40-0008-504
R33	Resistor, Fixed Composition, 33K ohms, 5%, 1/4W	81349	RCR07G333J
R34	Resistor, Fixed Composition, 39K ohms, 5%, 1/4W	81349	RCR07G393J
R36	Resistor, Fixed Composition, 12K ohms, 5%, 1/4W	81349	RCR07G123J
R37	Resistor, Fixed Composition, 33K ohms, 5%, 1/4W	81349	RCR07G333J
R38, R39	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R40	Resistor, Fixed Composition, 7500 ohms, 5%, 1/4W	81349	RCR07G752J
R41	Resistor, Fixed Composition, 12K ohms, 5%, 1/4W	81349	RCR07G123J
R42	Resistor, Fixed Composition, 3900 ohms, 5%, 1/4W	81349	RCR07G392J
R43, R44	Resistor, Fixed Composition, 1200 ohms, 5%, 1/4W	81349	RCR07G122J
S1	Switch, Slide, SPDT	14304	S30-0004-002
T1, T2	Transformer, Audio	14304	T30-0001-105
U1	Integrated Circuit, Quad 2-Input NAND Gate, Type CD4011AE	14304	I01-0031-000
U2	Integrated Circuit, Hex Inverter, Type CD4069UBE	14304	I02-0002-000
U3	Integrated Circiut, Phase Locked Loop, Type CD4046AE	14304	I65-0001-000
U4	Integrated Circuit, Dual-D Flip Flop, Type CD4013AE	14304	I05-0002-000
U5	Integrated Circuit, Phase Locked Loop, Type CD4046AE	14304	I65-0001-000
U6, U7	Integrated Circuit, Triple 3-Input NAND Gate, Type CD4023AE	14304	I01-0006-000
U8	Integrated Circuit, Quad Exclusive OR Gate, Type CD4030AE	14304	I01-0005-000
U9	Integrated Circuit, Dual 4-Input NOR Gate, Type CD4002AE	14304	I01-0004-000
U10	Integrated Circuit, Presettable Up/Down Counter, Type CD4029AE	14304	I41-0001-000

Table 6-2. MODULATOR PWB A1 PARTS LIST (Cont.)

Ref. Desig.	Name and Description	Mfr.	Part No.
U11	Integrated Circuit, Hex "D" Flip-Flop, Type MC14174BCP	14304	105-0009-000
U12	Integrated Circuit, Quad 2-Input NOR Gate, Type CD4001AE	14304	101-0003-000
U13	Integrated Circuit, Quad 2-Input NAND Gate, Type CD4011AE	14304	101-0031-000
U14	Integrated Circuit, Dual "D" Flip-Flop, Type CD4013AE	14304	105-0002-000
U15	Integrated Circuit, 8-Bit Binary/8 Stage Down Counter, Type CD40103BE	14304	141-0005-000
U16	Integrated Circuit, Hex "D" Flip-Flop, Type MC14174BCP	14304	105-0009-000
U17	Integrated Circuit, Dual 4 Stage Shift Register, Type CD4015AE	14304	155-0001-000
U18	Integrated Circuit, Quad 2-Input NOR Gate, Type CD4001AE	14304	101-0003-000
U19	Integrated Circuit, Dual "D" Flip-Flop, Type CD4013AE	14304	105-0002-000
U20	Integrated Circuit, Dual Monostable Multivibrator, Type CD4098BE	14304	105-0001-000
U21	Integrated Circuit, Presettable Up/Down Counter Type CD4029AE	14304	141-0001-000
U22	Integrated Circuit, Hex "D" Flip-Flop, Type MC14174BCP	14304	105-0009-000
U23	Integrated Circuit, Dual 4-Stage Static Shift Register Type CD4015AE	14304	155-0001-000
U24	Integrated Circuit, Dual "D" Flip-Flop, Type CD4013AE	14304	105-0002-000
U25	Integrated Circuit, Dual 4-Stage Static Shift Register Type CD4015AE	14304	155-0001-000
U26	Integrated Circuit, 8-Bit Binary/8 Stage Down Counter Type CD40103BE	14304	141-0005-000
U27	Integrated Circuit, Hex "D" Flip-Flop, Type MC14174 BCP	14304	105-0009-000
U28	Integrated Circuit, Dual 4-State Static Shift Register Type, CD4015AE	14304	155-0001-000
U29	Integrated Circuit, Decade Counter/Divider, Type CD4017AE	14304	141-0002-000
U30	Integrated Circuit, Resistor Network	14304	6918-1123
U31, U32	Integrated Circuit, Quad Op-Amp	14304	130-0013-000

Table 6-3. DEMODULATOR PWB A2 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
A2	Demodulator PWB Assembly	14304	6918-1130
	(Note: Prefix all reference designators with A2)		
C1	Capacitor, Tantalum, 1 uF, 10% Vdcw	14304	C25-0002-007
C2, C3	Capacitor, Mica, 82 pF, 5%, 500 Vdcw	81349	CM04ED820J03
C4	Capacitor, Tantalum, 1 uF, 10%, 50 Vdcw	14304	C25-0002-007
C5 - C12	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
C13 - C20	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C21	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
C22, C23	Capacitor, Tantalum, 10 uF, 10%, 50 Vdcw	14304	C25-0002-013
C24	Capacitor, Tantalum, 1 uF, 10%, 50 Vdcw	14304	C25-0002-007
C25	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
C26	Capacitor, Tantalum, 1 uF, 10%, 50 Vdcw	14304	C25-0002-007
C27	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
C28, C29	Capacitor, Tantalum, 10 uF, 10%, 50 Vdcw	14304	C25-0002-013
C30	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
C31, C32	Capacitor, Ceramic, .0068 uF, 5%, 100 Vdcw	14304	C11-0012-682
C33	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C34 - C36	Capacitor, Ceramic, .01 uF, 5%, 100 Vdcw	14304	C11-0012-103
C37, C38	Capacitor, Ceramic, .0068 uF, 5%, 100 Vdcw	14304	C11-0012-682
C39	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C40 - C42	Capacitor, Ceramic, .01 uF, 5%, 100 Vdcw	14304	C11-0012-103
C43	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
C44	Capacitor, Ceramic, .01 uF, 5%, 100 Vdcw	14304	C11-0012-103
C45	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
C46	Capacitor, Tantalum, 4.7 uF, 10%, 50 Vdcw	14304	C25-0002-011
C47, C48	Capacitor, Tantalum, 2.2 uF, 10%, 50 Vdcw	14304	C25-0002-009
C49, C50	Capacitor, Ceramic, .0056 uF, 5%, 100 Vdcw	14304	C11-0012-562
C51	Capacitor, Tantalum, 1 uF, 10%, 50 Vdcw	14304	C25-0002-007
C52	Capacitor, Tantalum, 2.2 uF, 10%, 50 Vdcw	14304	C25-0002-009
C53	Capacitor, Ceramic, .0056 uF, 5%, 100 Vdcw	14304	C11-0012-562
C54	Capacitor, Ceramic, .033 uF, 5%, 100 Vdcw	14304	C11-0012-333
C55	Capacitor, Ceramic, .001 uF, 5%, 100 Vdcw	14304	C11-0012-102
C56	Capacitor, Ceramic, .0022 uF, 5%, 100 Vdcw	14304	C11-0012-222
C57	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C58	Capacitor, Ceramic, .047 uF, 5%, 100 Vdcw	14304	C11-0012-473
C59	Capacitor, Ceramic, .001 uF, 5%, 100 Vdcw	14304	C11-0012-102
C60	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C61	Capacitor, Ceramic, .001 uF, 20%, 50 Vdcw	14304	C11-0005-102



NOTE: FOR COMPONENT IDENTIFICATION, PREFIX ALL REFERENCE DESIGNATIONS WITH A2.

Figure 6-3. Demodulator Pwb A2 Component Locations

Table 6-3. DEMODULATOR PWB A2 PARTS LIST (Cont.)

Ref. Desig.	Name and Description	Mfr.	Part No.
C62	Capacitor, Tantalum, 1 uF, 10%, 50 Vdcw	14304	C25-0002-007
C63	Capacitor, Ceramic, .0056 uF, 5%, 100 Vdcw	14304	C11-0012-526
C64	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
C65 - C80	Capacitor, Ceramic, .0047 uF, 5%, 100 Vdcw	14304	C11-0012-472
C81	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
C82 - C86	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C87, C88	Capacitor, Tantalum, 22 uF, 10%, 50 Vdcw	14304	C25-0002-015
C89	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
CR1 - CR3	Diode, Silicon, Type 1N4148	14304	D10-4148-000
CR3	Not Used		
CR5, CR6	Diode, Silicon, Type 1N4148	14304	D10-4148-000
CR7	Not Used		
CR8-CR16	Diode, Silicon, Type 1N4148	14304	D10-4148-000
J1, J	Not Used		
J3, J4	Connector	14304	J25-0008-005
P1	Connector, Socket	14304	J25-0001-005
Q1	Transistor, PNP Type	14304	Q02-2907-000
Q2, Q3	Transistor, FET	14304	Q02-4391-000
R1	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R2	Resistor, Fixed Composition 1500 ohms, 5%, 1/4W	81349	RCR07G152J
R3	Resistor, Fixed Composition, 68K ohms, 5% 1/4W	81349	RCR07G683J
R4, R5	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R6	Resistor, Fixed Composition, 1500 ohms, 5%, 1/4W	81349	RCR07G152J
R7	Resistor, Fixed Composition, 68K ohms, 5%, 1/4W	81349	RCR07G683J
R8	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R9, R10	Resistor, Fixed Composition, 33K ohms, 5%, 1/4W	81349	RCR07G333J
R11	Not Used		
R12	Resistor, Fixed Composition, 7500 ohms, 5%, 1/4W	81349	RCR07G752J
R13-R16	Resistor, Fixed Composition, 2200 ohms, 5%, 1/4W	81349	RCR07G222J
R17	Resistor, Fixed Composition, 470 ohms, 5%, 1/4W	81349	RCR07G471J
R18	Resistor, Fixed Composition, 24K ohms, 5%, 1/4W	81349	RCR07G243J
R19	Resistor, Variable, 20K ohms	14304	R40-0008-203
R20	Resistor, Fixed Composition, 470 ohms, 5%, 1/4W	81349	RCR07G471J
R21	Resistor, Fixed Composition, 24K ohms, 5%, 1/4W	81349	RCR07G243J
R22	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R23	Resistor, Fixed Composition, 2200 ohms, 5%, 1/4W	81349	RCR07G222J
R24, R25	Resistor, Fixed Composition, 3000 ohms, 5%, 1/4W	81349	RCR07G302J
R26, R27	Resistor, Fixed Composition, 56K ohms, 5%, 1/4W	81349	RCR07G563J

Table 6-3. DEMODULATOR PWB A2 PARTS LIST (Cont.)

Ref. Desig.	Name and Description	Mfr.	Part No.
R28, R29	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R30	Resistor, Fixed Composition, 5100 ohms, 5%, 1/4W	81349	RCR07G512J
R31	Resistor, Variable, 500 ohms	14304	R40-0008-501
R32	Resistor, Fixed Composition, 7500 ohms, 5%, 1/4W	81349	RCR07G752J
R33-R36	Resistor, Fixed Composition, 2200 ohms, 5%, 1/4W	81349	RCR07G222J
R37	Resistor, Fixed Composition, 470 ohms, 5%, 1/4W	81349	RCR07G471J
R38	Resistor, Fixed Composition, 24K ohms, 5%, 1/4W	81349	RCR07G243J
R39	Resistor, Fixed Composition, 470 ohms, 5%, 1/4W	81349	RCR07G471J
R40	Resistor, Fixed Composition, 24K ohms, 5%, 1/4W	81349	RCR07G243J
R41	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R42	Resistor, Fixed Composition, 2200 ohms, 5%, 1/4W	81349	RCR07G222J
R43, R44	Resistor, Fixed Composition, 3000 ohms, 5%, 1/4W	81349	RCR07G302J
R45, R46	Resistor, Fixed Composition, 56K ohms, 5%, 1/4W	81349	RCR07G563J
R47, R48	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R49	Resistor, Fixed Composition, 5100 ohms, 5%, 1/4W	81349	RCR07G512J
R50	Resistor, Variable, 20K ohms	14304	R40-0008-203
R51	Resistor, Fixed Composition, 51 ohms, 5%, 1/4W	81349	RCR07G510J
R52	Resistor, Variable 500 ohms	14304	R40-0008-501
R53, R54	Resistor, Fixed Composition, 2700 ohms, 5%, 1/4W	81349	RCR07G272J
R55	Resistor, Fixed Composition, 30K ohms, 5%, 1/4W	81349	RCR07G303J
R56	Resistor, Fixed Composition, 68K ohms, 5%, 1/4W	81349	RCR07G683J
R57	Resistor, Fixed Composition, 12K ohms, 5%, 1/4W	81349	RCR07G123J
R58	Resistor, Fixed Composition, 51 ohms, 5%, 1/4W	81349	RCR07G510J
R59	Resistor, Variable, 100 ohms	14304	R40-0008-101
R60	Resistor, Fixed Composition, 39K ohms, 5%, 1/4W	81349	RCR07G393J
R61	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R62	Resistor, Fixed Composition, 15K ohms, 5%, 1/4W	81349	RCR07G153J
R63	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R64	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R65	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R66	Resistor, Fixed Composition, 8200 ohms, 5%, 1/4W	81349	RCR07G822J
R67	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R68, R69	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R70, R71	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R72	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R73	Resistor, Fixed Composition, 51 ohms, 5%, 1/4W	81349	RCR07G510J
R74	Resistor, Variable, 500 ohms	14304	R40-0008-501
R75, R76	Resistor, Fixed Composition, 2700 ohms, 5%, 1/4W	81349	RCR07G272J

Table 6-3. DEMODULATOR PWB A2 PARTS LIST (Cont.)

Ref. Desig.	Name and Description	Mfr.	Part No.
R77	Resistor, Fixed Composition, 30K ohms, 5% 1/4W	81349	RCR07G303J
R78	Resistor, Fixed Composition, 68K ohms, 5%, 1/4	81349	RCR07G683J
R79	Resistor, Fixed Composition, 12K ohms, 5%, 1/4W	81349	RCR07G123J
R80	Resistor, Fixed Composition, 51 ohms, 5%, 1/4W	81349	RCR07G510J
R81	Resistor, Variable, 100 ohms	14304	R40-0008-101
R82	Resistor, Fixed Composition, 39K ohms, 5%, 1/4W	81349	RCR07G393J
R83	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R84	Resistor, Fixed Composition, 15K ohms, 5%, 1/4W	81349	RCR07G153J
R85	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R86	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R87	Resistor, Fixed Composition, 8200 ohms, 5%, 1/4W	81349	RCR07G822J
R88	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R89	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R90	Resistor, Fixed Composition, 8200 ohms, 5%, 1/4W	81349	RCR07G822J
R91	Resistor, Fixed Composition, 1000 ohms, 5%, 1/4W	81349	RCR07G102J
R92	Resistor, Fixed Composition, 220K ohms, 5%, 1/4W	81349	RCR07G224J
R93	Not Used		
R94	Resistor, Fixed Composition, 6200 ohms, 5%, 1/4W	81349	RCR07G622J
R95	Resistor, Fixed Composition, 5600 ohms, 5%, 1/4W	81349	RCR07G562J
R96	Resistor, Fixed Composition, 100 ohms, 5%, 1/4W	81349	RCR07G101J
R97	Resistor, Fixed Composition, 150K ohms, 5%, 1/4W	81349	RCR07G154J
R98	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R99	Resistor, Fixed Composition, 6200 ohms, 5%, 1/4W	81349	RCR07G622J
R100	Resistor, Fixed Composition, 5600 ohms, 5%, 1/4W	81349	RCR07G562J
R101	Resistor, Fixed Composition, 200 ohms, 5%, 1/4W	81349	RCR07G201J
R102	Resistor, Fixed Composition, 3000 ohms, 5%, 1/4W	81349	RCR07G302J
R103	Resistor, Fixed Composition, 3900 ohms, 5%, 1/4W	81349	RCR07G392J
R104	Resistor, Fixed Composition, 560K ohms, 5%, 1/4W	81349	RCR07G564J
R105	Resistor, Fixed Composition, 120K ohms, 5%, 1/4W	81349	RCR07G124J
R106	Resistor, Fixed Composition, 1000 ohms, 5%, 1/4W	81349	RCR07G102J
R107	Resistor, Fixed Composition, 22K ohms, 5%, 1/4W	81349	RCR07G223J
R108	Resistor, Fixed Composition, 9100 ohms, 5%, 1/4W	81349	RCR07G912J
R109	Resistor, Fixed Composition, 2400 ohms, 5%, 1/4W	81349	RCR07G242J
R110	Resistor, Fixed Composition, 10 Meg ohms, 5%, 1/4W	81349	RCR07G106J
R111-112	Resistor, Fixed Composition, 3600 ohms, 5%, 1/4W	81349	RCR07G362J
R113-114	Resistor, Fixed Composition, 15K ohms, 5%, 1/4W	81349	RCR07G153J
R115	Resistor, Fixed Composition, 27K ohms, 5%, 1/4W	81349	RCR07G273J
R116	Resistor, Fixed Composition, 4700 ohms, 5%, 1/4W	81349	RCR07G472J

Table 6-3. DEMODULATOR PWB A2 PARTS LIST (Cont.)

Ref. Desig.	Name and Description	Mfr.	Part No.
R117	Resistor, Fixed Composition, 2700 ohms, 5%, 1/4W	81349	RCR07G272J
R118	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R119	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R120	Resistor, Fixed Composition, 22K ohms, 5%, 1/4W	81349	RCR07G223J
R121	Resistor, Fixed Composition, 680K ohms, 5%, 1/4W	81349	RCR07G684J
R122	Resistor, Fixed Composition, 16K ohms, 5%, 1/4W	81349	RCR07G163J
R123	Resistor, Fixed Composition, 22K ohms, 5%, 1/4W	81349	RCR07G223J
R124	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R125	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R126	Not Used		
R127	Resistor, Fixed Composition, 2000 ohms, 5%, 1/4W	81349	RCR07G202J
R128	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R129	Resistor, Fixed Composition, 2000 ohms, 5%, 1/4W	81349	RCR07G202J
R130	Resistor, Fixed Composition, 510 ohms, 5%, 1/4W	81349	RCR07G511J
R131	Resistor, Variable, 1000 ohms	14304	R30-0008-102
R132	Resistor, Fixed Composition, 1200 ohms, 5%, 1/4W	81349	RCR07G122J
R133	Resistor, Fixed Composition, 6800 ohms, 5%, 1/4W	81349	RCR07G682J
R134	Resistor, Fixed Composition, 2000 ohms, 5%, 1/4W	81349	RCR07G202J
R135	Resistor, Fixed Composition, 2400 ohms, 5%, 1/4	81349	RCR07G242J
R136	Resistor, Variable, 5000 ohms	14304	R30-0008-502
R137,138	Resistor, Fixed Composition, 300 ohms, 5%, 1/4W	81349	RCR07G301J
R139	Resistor, Fixed Composition, 1000 ohms, 5%, 1/4W	81349	RCR07G102J
R140	Resistor, Fixed Composition, 5100 ohms, 5%, 1/4W	81349	RCR07G512J
R141	Resistor, Fixed Composition, 18K ohms, 5%, 1/4W	81349	RCR07G183J
R142	Resistor, Fixed Composition, 47K ohms, 5%, 1/4W	81349	RCR07G473J
R143	Resistor, Fixed Composition, 16K ohms, 5%, 1/4W	81349	RCR07G163J
R144	Resistor, Fixed Composition, 18K ohms, 5%, 1/4W	81349	RCR07G183J
R145	Resistor, Fixed Composition, 13K ohms, 5%, 1/4W	81349	RCR07G133J
R146	Resistor, Fixed Composition, 1000 ohms, 5%, 1/4W	81349	RCR07G102J
R147	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R148	Resistor, Fixed Composition, 13K ohms, 5%, 1/4W	81349	RCR07G133J
R149	Resistor, Fixed Composition, 5600 ohms, 5%, 1/4W	81349	RCR07G562J
R150	Resistor, Fixed Composition, 6200 ohms, 5%, 1/4W	81349	RCR07G622J
R151	Resistor, Fixed Composition, 5600 ohms, 5%, 1/4W	81349	RCR07G562J
R152,153	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R154,155	Resistor, Fixed Composition, 200 ohms, 5%, 1/4W	81349	RCR07G201J
R156	Resistor, Fixed Composition, 24K ohms, 5%, 1/4W	81349	RCR07G243J
R157	Resistor, Fixed Composition, 820K ohms, 5%, 1/4W	81349	RCR07G824J

Table 6-3. DEMODULATOR PWB A2 PARTS LIST

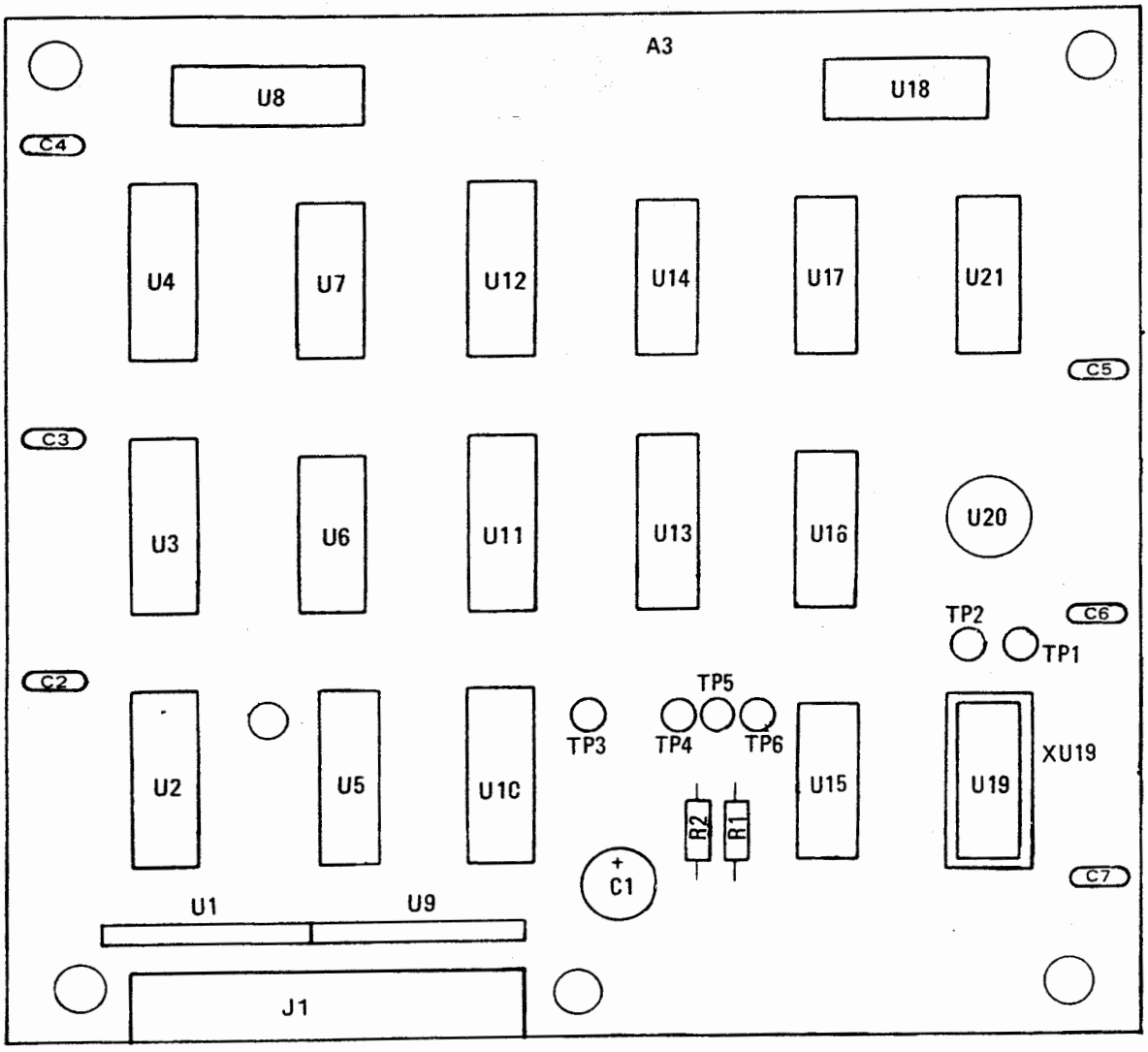
Ref. Desig.	Name and Description	Mfr.	Part No.
R158	Resistor, Fixed Composition, 51K ohms, 5%, 1/4W	81349	RCR07G513J
R159	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R160	Resistor, Fixed Composition, 6200 ohms, 5%, 1/4W	81349	RCR07G622J
R161	Resistor, Fixed Composition, 120K ohms, 5%, 1/4W	81349	RCR07G124J
R162	Resistor, Fixed Composition, 5600 ohms, 5%, 1/4W	81349	RCR07G562J
R163	Resistor, Fixed Composition, 200 ohms, 5%, 1/4W	81349	RCR07G201J
R164	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R165	Resistor, Fixed Composition, 33K ohms, 5%, 1/4W	81349	RCR07G333J
R166	Resistor, Variable, 5000 ohms	14304	R40-0008-502
R167	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R168	Resistor, Fixed Composition, 24K ohms, 5%, 1/4W	81349	RCR07G243J
R169	Resistor, Fixed Composition, 12K ohms, 5%, 1/4W	81349	RCR07G123J
R170	Resistor, Fixed Composition, 7500 ohms, 5%, 1/4W	81349	RCR07G752J
R171	Resistor, Fixed Composition, 2000 ohms, 5%, 1/4W	81349	RCR07G202J
R172,173	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
T1	Transformer	14304	T30-0001-105
U1, U2	Integrated Circuit, Dual 4-Stage Shift Register, Type CD4015AE	14304	I55-0001-000
U3, U4	Integrated Circuit Hex D Flip-Flop, Type MD14174BCP	14304	I05-0009-000
U5	Integrated Circuit, Presettable Up/Down Counter Type CD4029Ae	14304	I41-0001-000
U6	Integrated Circuit, 8 Bit Down Counter, Type CD40103BE	14304	I41-0005-000
U7	Integrated Circuit, Hex D Flip-Flop, Type MD14174BCP	14304	I05-0009-000
U8	Integrated Circuit, Dual 4-Stage Shift Register, Type CD4015AE	14304	I55-0001-000
U9	Integrated Circuit, Presettable Up/Down Counter Type CD4029AE	14304	I41-0001-000
U10	Integrated Circuit, Hex D Flip-Flop, Type MC14174BCP	14304	I05-0009-000
U11	Integrated Circuit, Dual 4-Input NOR Gate, Type CD4002AE	14304	I01-0004-000
U12	Integrated Circuit, 8-Bit Down Counter, Type CD40103BE	14304	I41-0005-000
U13	Integrated Circuit, Dual D Flip-Flop, Type CD4013AE	14304	I05-0002-000
U14	Integrated Circuit, Hex Inverter, Type CD4069BE	14304	I02-0002-000
U15, U16	Integrated Circuit, Phase Locked Loop, Type CD4046AE	14304	I65-0001-000

Table 6-3. DEMODULATOR PWB A2 PARTS LIST (Cont.)

Ref. Desig.	Name and Description	Mfr.	Part No.
U17 - U20	Integrated Circuit, Decade Counter/Divider, Type CD4017AE	14304	I41-0002-000
U21	Integrated Circuit, Quad 2-Input NAND Gate, Type CD4011AE	14304	I01-0031-000
U22	Integrated Circuit, 12 Stage Ripple Counter, Type CD4040AE	14304	I41-0007-000
U23	Integrated Circuit, Dual D Flip-Flop, Type CD4013AE	14304	I05-0002-000
U24	Integrated Circuit, Triple 3-Input NAND Gate, Type CD4023AE	14304	I01-0006-000
U25	Integrated Circuit, Quad Exclusive OR Gate, Type CD4030AE	14304	I01-0005-340
U26	Integrated Circuit, Dual D Flip-Flop, Type CD4013AE	14304	I05-0002-000
U27	Integrated Circuit, Quad 2-Input NOR Gate, Type CD4001AE	14304	I01-0003-000
U28	Integrated Circuit, Quad 2-Input NAND Gate, Type CD4011AE	14304	I01-0031-000
U29	Integrated Circuit, Dual D Flip-Flop, Type CD4013AE	14304	I05-0002-000
U30	Integrated Circuit, 12 Stage Ripple Counter, Type CD4040AE	14304	I41-0007-000
U31	Integrated Circuit, Dual D Flop-Flop, Type CD4013AE	14304	I05-0002-000
U32	Integrated Circuit, Dual 4-Stage Shift Register, Type CD4015AE	14304	I55-0001-000
U33	Integrated Circuit, Presettable Up/Down Counter Type CD4029AE	14304	I41-0001-000
U34	Integrated Circuit, Balanced Modulator/Demodulator Type MC1496P	14304	I62-0001-000
U35 - U38	Integrated Circuit, Quad Operational Amplifier, Type HA1-4741-5	14304	I30-0013-000
U39	Integrated Circuit, Voltage Comparator, Type LM399	14304	I20-0006-000
U40, U41	Integrated Circuit, Sample and Hold, Type LF398H	14304	I54-0001-000
U42	Not Used		
U43, U44	Integrated Circuit, Multiplexer/Demultiplexer, Type CD4051BE	14304	I09-0003-000
U45 - U47	Integrated Circuit, Quad Operational Amplifier, Type HA1-4741-5	14304	I30-0013-000
U48	Integrated Circuit, Balanced Modulator/Demodulator	14304	I62-0001-000
VR1, VR2	Voltage Regulator, 3.3V	14304	D30-0047-933
W1	Cable, Flat 28 AWG	14304	W55-0001-008

Table 6-4. TIMING/CONTROL PWB A3 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
A3	Timing/Control PWB Assembly (Note: Prefix all reference designators with A3)	14304	6918-1140
C1	Capacitor, Tantalum, 22 uF, 10%, 50 Vdcw	14304	C25-0002-015
C2 to C7	Capacitor, Ceramic, .01 uF, 20%, 50 Vdcw	14304	C11-0005-103
R1, R2	Resistor, Fixed Composition, 33K ohms, 5%, 1/4W	81349	RCR07G333J
U1	Integrated Circuit, Resistor Network, 33K ohms	14304	R50-0010-333
U2	Integrated Circuit, Presettable 8-Bit Down Counter Type CD40102BE	14304	I41-0004-000
U3, U4	Integrated Circuit, 8 Stage Static Shift Register Type CD4021AE	14304	I55-0002-000
U5	Integrated Circuit, Presettable Up/Down Counter Type CD4029AE	14304	I41-0001-000
U6	Integrated Circuit, Triple 3-Input NAND Gate, Type CD4023AE	14304	I01-0006-000
U7	Integrated Circuit, 7 Stage Binary Counter, Type CD4024AE	14304	I41-0003-000
U8	Integrated Circuit, 12 Stage Counter/Divider, Type CD4040AE	14304	I41-0007-000
U9	Integrated Circuit, Resistor Network, 33K ohms	14304	R50-0010-333
U10	Integrated Circuit, Presettable Down Counter, Type CD40102BE	14304	I41-0004-000
U11	Integrated Circuit, Positive Triple Serial Adder, Type CD4032AE	14304	I42-0001-000
U12	Integrated Circuit, 8 Stage Static Shift Register Type CD4021AE	14304	I55-0002-000
U13	Integrated Circuit, Negative Triple Serial Adder Type CD4038AE	14304	I42-0002-000
U14	Integrated Circuit, Hex Inverter, Type CD4069UBE	14304	I02-0002-000
U15, U16	Integrated Circuit, 7 Stage Binary Counter, Type CD4024AE	14304	I41-0003-000
U17	Integrated Circuit, Quad 2-Input NOR Gate, Type CD4001AE	14304	I01-0003-000
U18	Integrated Circuit, Dual D Flip-Flop, Type CD4013AE	14304	I05-0002-000
U19	Integrated Circuit, 7 Stage Binary Counter, Type CD4024AE	14304	I41-0003-000
U20	Integrated Circuit, 1.024 MHz, 12V Oscillator	14304	6918-1142
U21	Integrated Circuit, Dual D Flip-Flop, Type CD4013AE	14304	I05-0002-000
XU19	Socket, 14 Pin	14304	J75-0014-000

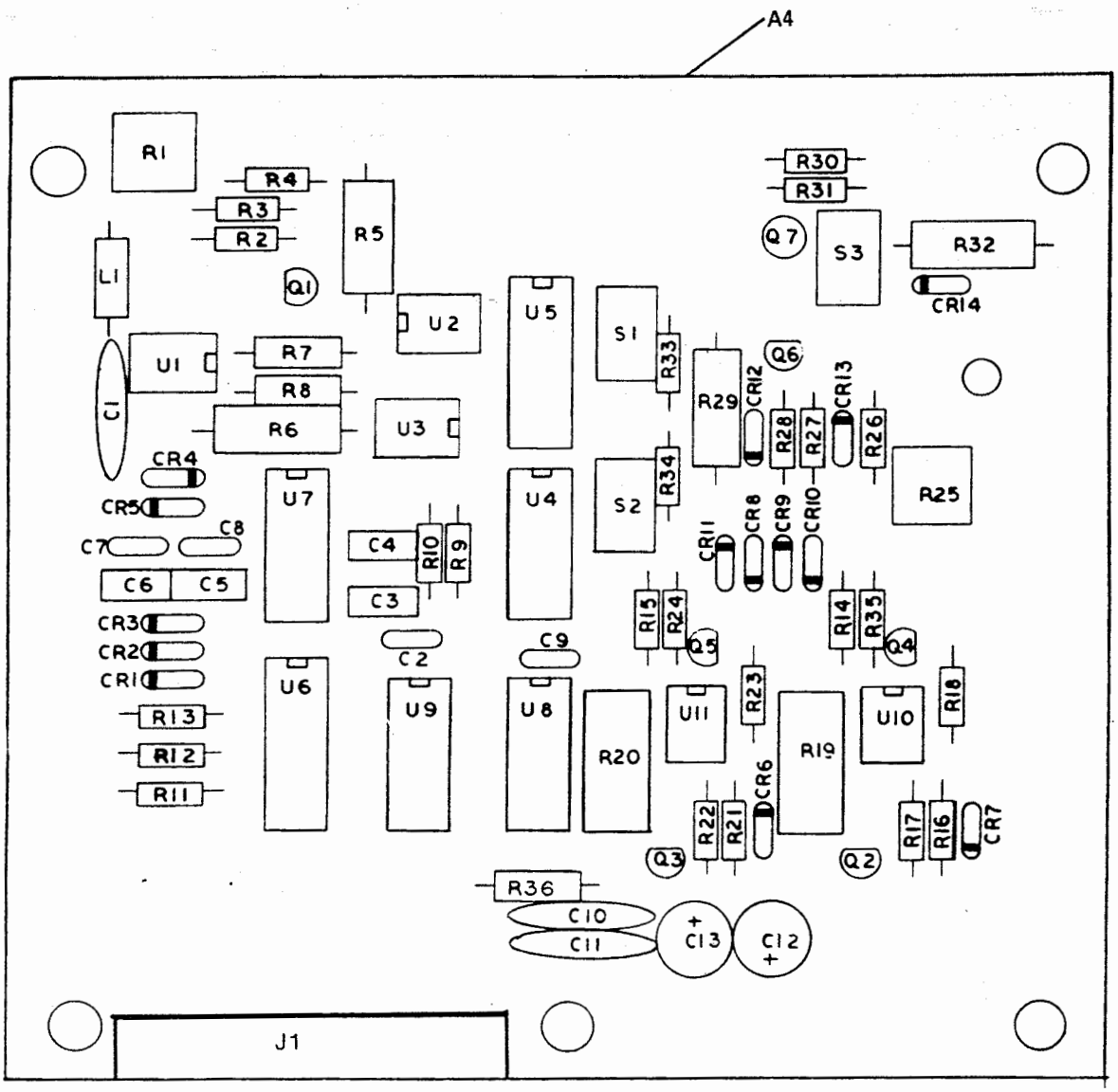


NOTE: FOR COMPONENT IDENTIFICATION, PREFIX ALL REFERENCE DESIGNATIONS WITH A3.

Figure 6-4. Timing and Control Pwb A3 Component Locations

Table 6-5. INTERFACE PWB A4 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
A4	Interface PWB Assembly	14304	6918-1150
	(Note: Prefix all reference designators with A4)		
C1	Capacitor, Ceramic, 3300 pF, 20%, 500 Vdcw	14304	C11-0002-332
C2	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C3 to C6	Capacitor, Ceramic, 330 pF, 10%, 50 Vdcw	14304	C11-0007-331
C7 to C9	Capacitor, Ceramic, .1 uF, 20%, 50 Vdcw	14304	C11-0005-104
C10, C11	Capacitor, Ceramic, 3300 pF, 20%, 500 Vdcw	14304	C11-0002-332
C12, C13	Capacitor, Tantalum, 22 uF, 10%, 50 Vdcw	14304	C25-0002-015
CR1 - CR3	Diode, Germanium, Type 1N277	14304	C10-0277-000
CR4, CR5	Diode, Silicon, Type 1N4148	14304	C10-4148-000
CR6-CR14	Diode, Silicon, Rectifier	14304	D22-0001-000
L1	Choke, 220 uH, 5%	81349	LT10K020
Q1	Transistor, NPN Type	14304	Q02-6515-000
Q2	Transistor, PNP Type	14304	Q02-6518-000
Q3, Q4	Transistor, NPN Type	14304	Q02-6515-000
Q5	Transistor, PNP Type	14304	Q02-6518-000
Q6	Transistor, NPN Type	14304	Q02-6515-000
Q7	Transistor, PNP Type	14304	Q02-2907-000
R1	Resistor, Variable 1000 ohms	14304	R40-0007-102
R2	Resistor, Fixed Composition, 4.7 ohms, 5%, 1/4W	81349	RCR07G4R7J
R3	Resistor, Fixed Composition, 6.8 ohms, 5%, 1/4W	81349	RCR07G6R8J
R4	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R5	Resistor, Fixed Composition, 30K ohms, 5%, 1W	81349	RCR32G303J
R6	Resistor, Fixed Composition, 270 ohms, 5%, 1W	81349	RCR32G271J
R7, R8	Resistor, Fixed Composition, 120 ohms, 5%, 1/2W	81349	RCR20G121J
R9, R10	Resistor, Fixed Composition, 2000 ohms, 5%, 1/4W	81349	RCR07G202J
R11 - R13	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
R14, R15	Resistor, Fixed Composition, 680 ohms, 5%, 1/4W	81349	RCR07G681J
R16	Resistor, Fixed Composition, 270K ohms, 5%, 1/4W	81349	RCR07G274J
R17	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R18	Resistor, Fixed Composition, 2200 ohms, 5%, 1/4W	81349	RCR07G222J
R19, R20	Resistor, Fixed Composition, 10K ohms, 5%, 2W	81349	RCR42G103J
R21	Resistor, Fixed Composition, 270K ohms, 5%, 1/4W	81349	RCR07G274J
R22	Resistor, Fixed Composition, 20K ohms, 5%, 1/4W	81349	RCR07G203J
R23	Resistor, Fixed Composition, 2200 ohms, 5%, 1/4W	81349	RCR07G222J
R24	Resistor, Fixed Composition, 120K ohms, 5%, 1/4W	81349	RCR07G124J
R25	Resistor, Variable, 1000 ohms	14304	R40-0007-102
R26	Resistor, Fixed Composition, 4.7 ohms, 5%, 1/4W	81349	RCR07G4R7J



NOTE: FOR COMPONENT IDENTIFICATION, PREFIX ALL REFERENCE DESIGNATIONS WITH A4.

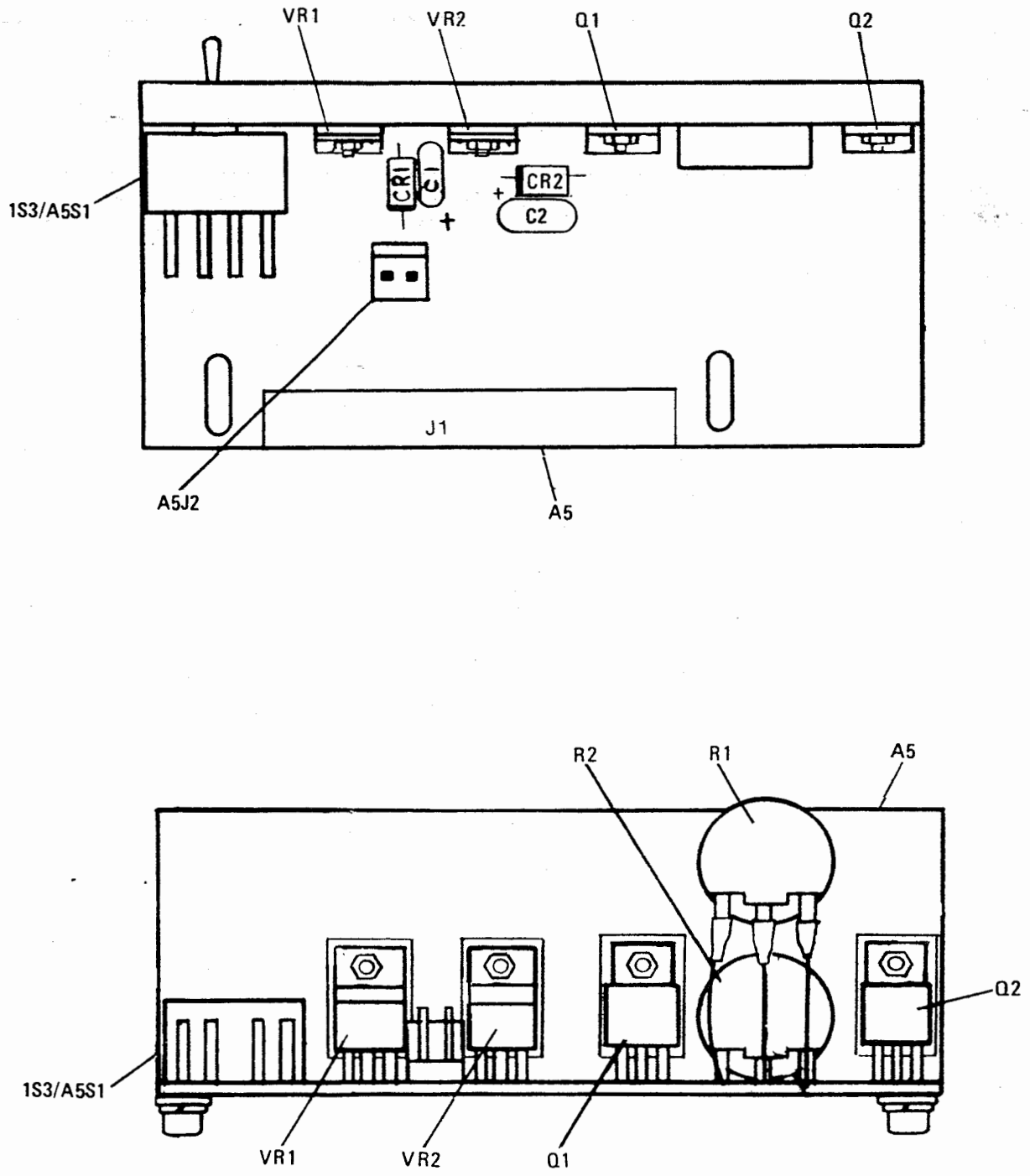
Figure 6-5. Interface Pwb A4 Component Locations

Table 6-5. INTERFACE PWB A4 PARTS LIST (Cont.)

Ref. Desig.	Name and Description	Mfr.	Part No.
R27	Resistor, Fixed Composition, 6.8 ohms, 5%, 1/4W	81349	RCR07G6R8J
R28	Resistor, Fixed Composition, 10K ohms, 5%, 1/4W	81349	RCR07G103J
R29	Resistor, Fixed Composition, 30K ohms, 5%, 1W	81349	RCR32G303J
R30	Resistor, Fixed Composition, 2700 ohms, 5%, 1/4W	81349	RCR07G272J
R31	Resistor, Fixed Composition, 4700 ohms, 5%, 1/4W	81349	RCR07G472J
R32	Resistor, Fixed Composition, 100 ohms, 5%, 1W	81349	RCR32G101J
R33, R34	Resistor, Fixed Composition, 33K ohms, 5%, 1/4W	81349	RCR07G333J
R35	Resistor, Fixed Composition, 120K ohms, 5%, 1/4W	81349	RCR07G124J
R36	Resistor, Fixed Composition, 22 ohms, 5%, 1/2W	81349	RCR20G220J
S1 to S3	Switch, Slide, SPDT	14304	S30-0004-002
U1	Integrated Circuit, Bridge Rectifier	14304	D22-5005-000
U2, U3	Integrated Circuit, Optoisolator, Type 4N35	14304	I75-0003-000
U4	Integrated Circuit, Quad 2-Input NAND Gate, Type CD4011AE	14304	I01-0031-000
U5	Integrated Circuit, Dual 4 Channel Data Selector, Type MC14539CP	14304	I15-0001-000
U6	Integrated Circuit, Hex Buffer/Converter, Inverting Type, CD4049Be	14304	I02-0011-000
U7	Integrated Circuit, Quad MDTL Line Driver, Type MC1488L	14304	I16-0001-000
U8	Integrated Circuit, Quad MDTL Line Receiver, Type MC1489L	14304	I17-0001-000
U9	Integrated Circuit, Hex Inverter, Type CD4069BE	14304	I02-0002-000
U10, U11	Integrated Circuit, Optoisolator, Type 4N35	14304	I75-0003-000

Table 6-6. TRANSISTOR/REGULATOR PWB A5 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
A5	Transistor/Regulator PWB Assembly	14304	6918-1190
	(Note: Prefix all reference designators with A5)		
C1, C2	Capacitor, Tantalum, 1 uF, 10%, 50 Vdcw	14304	C25-0002-007
CR1, CR2	Diode, Silicon	14304	D22-0001-000
J2	Header, 2 Pin	14304	J46-0012-002
Q1, Q2	Transistor, NPN Type	14304	Q20-0001-000
R1, R2	Resistor, Variable, 100 ohms, 2W	14304	R40-0010-101
S1	Switch, Toggle	14304	S10-0024-112
VR1	Integrated Circuit, +12 Volt Regulator, Type MC7912CT	14304	I12-0002-004
VR2	Integrated Circuit, +12 Volt Regulator, Type MC7812CT	14304	I12-0001-004

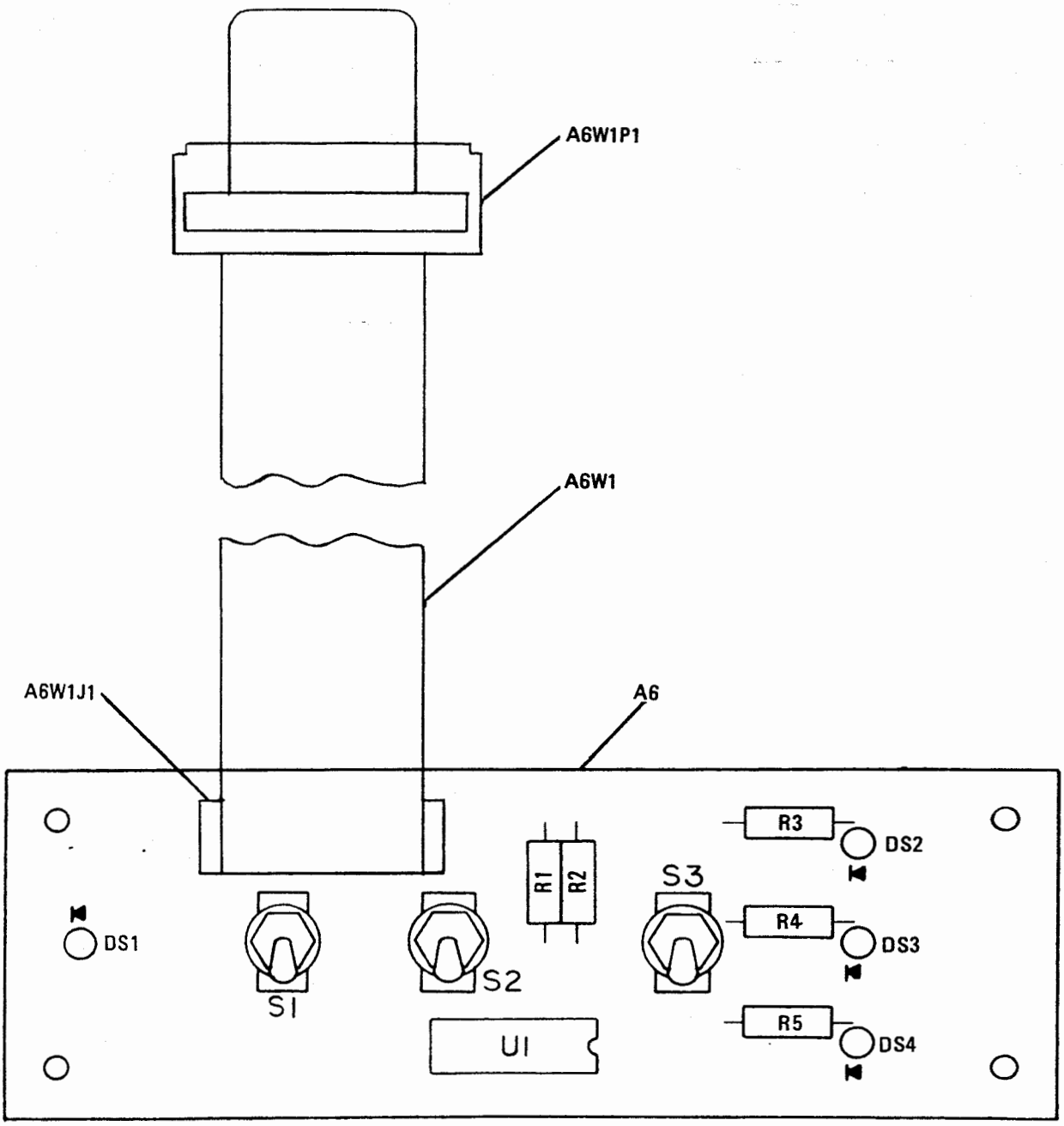


NOTE: FOR COMPONENT IDENTIFICATION, PREFIX ALL REFERENCE DESIGNATIONS WITH A5.

Figure 6-6. Transistor/Regulator Pwb A5 Component Locations

Table 6-7. CONTROL AND INDICATOR PWB A6 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
A6	Control and Indicator PWB Assembly (Note: Prefix all reference designators with A6)	14304	6918-1210
DS1 - DS4	Diode, LED	14304	N22-0001-000
J1	Connector, 20 Pin	14304	J25-0008-005
P1	Socket, 20 Pin	14304	J25-0001-002
R1, R2	Resistor, Fixed Composition, 33K ohms, 5%, 1/4W	81349	RCR07G333J
R3 - R5	Resistor, Fixed Composition, 430 ohms, 5%, 1/2W	81349	RCR20G431J
S1 - S3	Switch, Toggle, SPDT	14304	S10-0005-001
U1	Integrated Circuit Hex Inverter/Buffer	14304	I02-0001-000
W1	Cable, Flat	14304	W55-0001-004



NOTE: FOR COMPONENT IDENTIFICATION, PREFIX ALL REFERENCE DESIGNATIONS WITH A6.

Figure 6-7. Control and Indicator Pwb A6 Component Locations

Table 6-8. FREQUENCY CONTROL BOARD A7 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
A7	Frequency Control Board Assembly (Note: Prefix all reference designators with A7)	14304	6918-1220
J1	Connector, 26 Pin	14304	J25-0008-002
P1	Socket, 26 Pin	14304	J25-0001-003
S1	Switch, Thumbwheel	14304	6918-1222
W1	Cable, Flat, 26 Conductor	14304	W55-0001-006

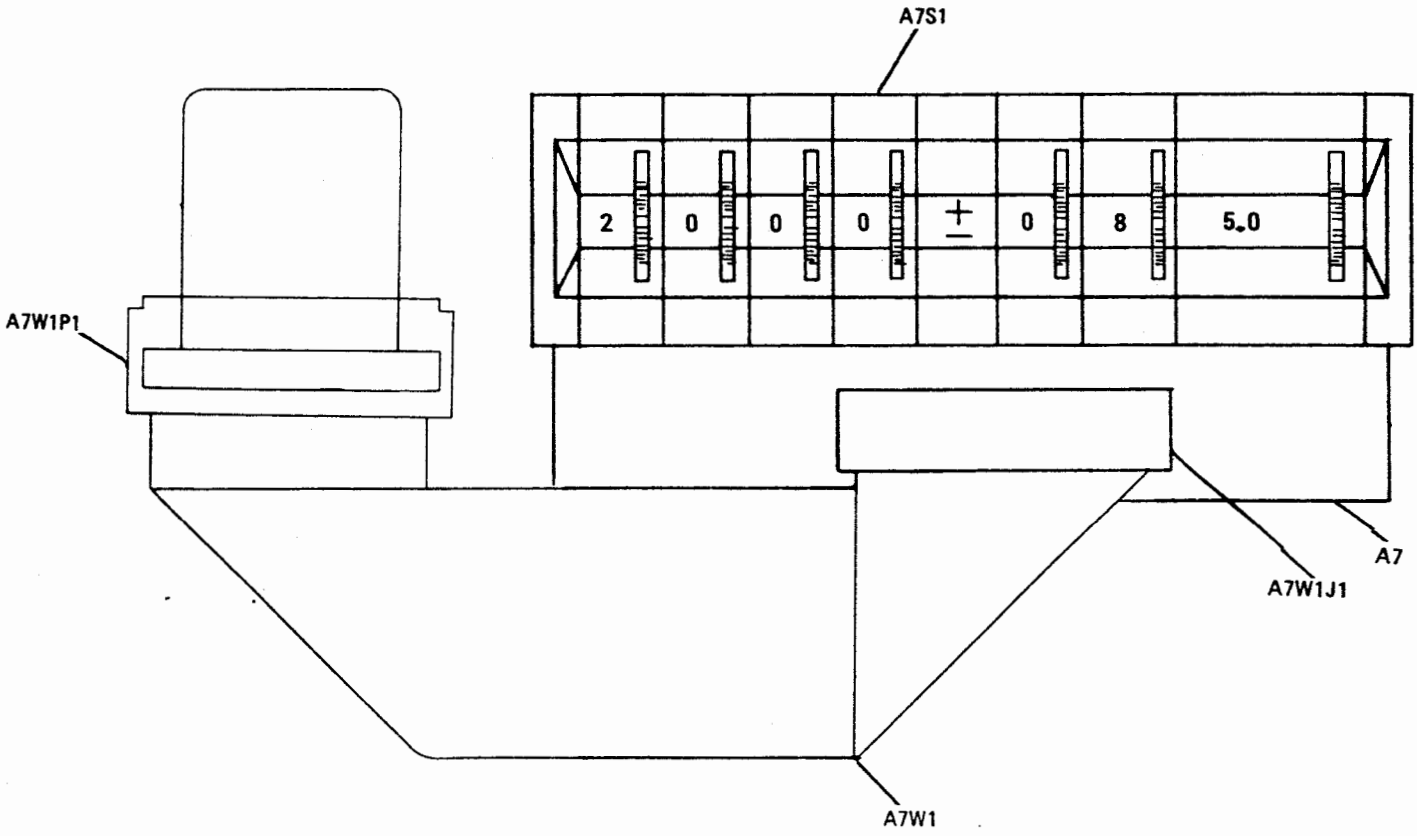
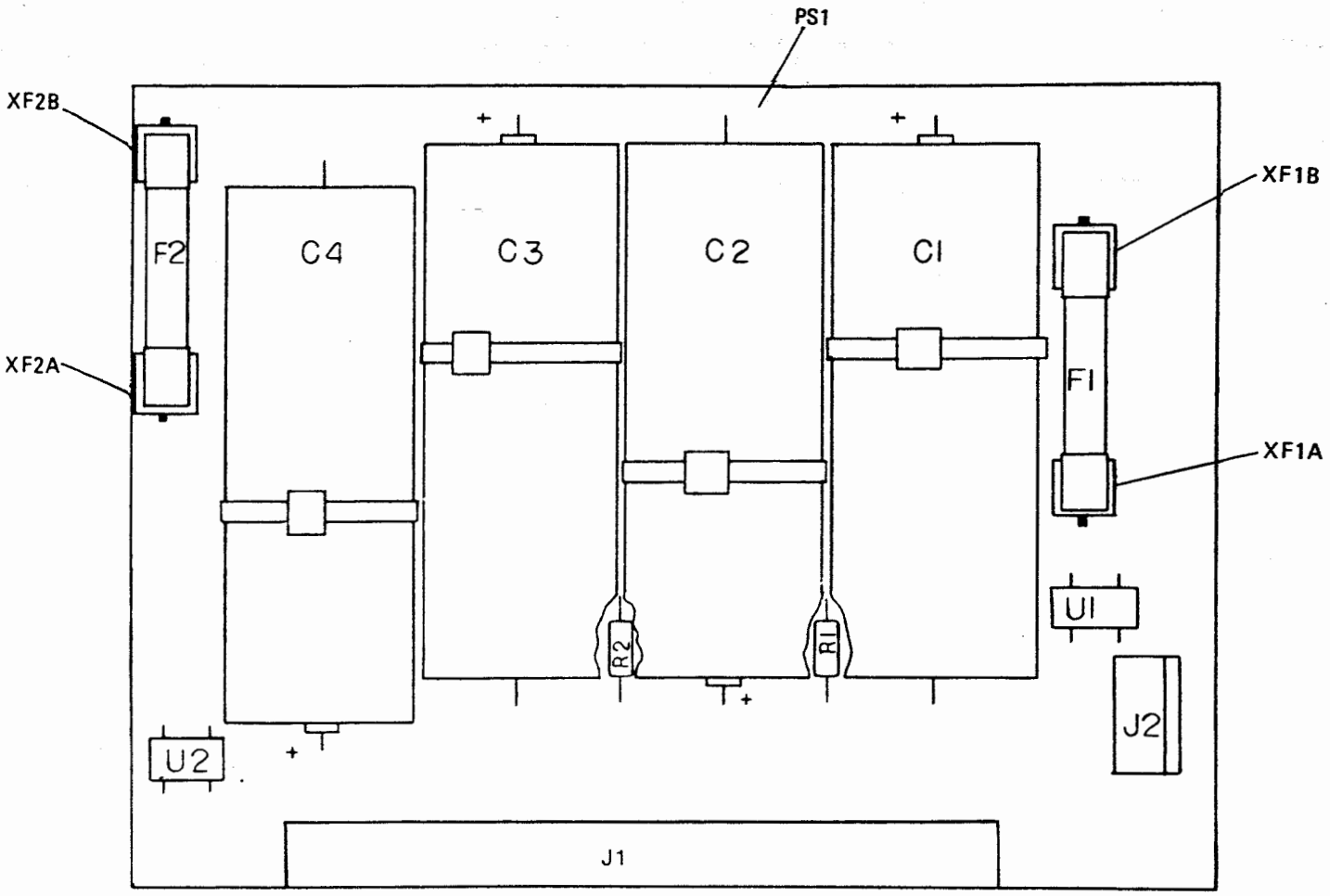


Figure 6-8. Frequency Control Board A7 Component Locations

Table 6-9. POWER SUPPLY PWB PS1 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
PS1	Power Supply PWB Assembly	14304	6918-1160
	(Note: Prefix all reference designators with PS1)		
C1, C2	Capacitor, Electrolytic, 400 uF, 100 Vdcw	14304	C20-0011-002
C3, C4	Capacitor, Electrolytic, 2000 uF, 35 Vdcw	14304	C20-0011-001
F1, F2	Fuse, 1/8 Amp, 250V	81349	F02A250V1/8AS
J2	Header, Straight Locking	14304	J46-0012-006
R1, R2	Resistor, Fixed Composition, 100K ohms, 5%, 1/4W	81349	RCR07G104J
U1, U2	Bridge Rectifier	14304	D22-5005-000
XF1A, XF1B, XF2A, XF2B.	Fuseholder, PWB Fuse Clip	14304	Z19-0009-000



NOTE: FOR COMPONENT IDENTIFICATION, PREFIX ALL REFERENCE DESIGNATIONS WITH PS1.

Figure 6-9. Power Supply Pwb PS1 Component Locations

Table 6-10. INTERCONNECTION PWB W1 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
W1	Interconnection PWB Assembly (Note: Prefix all reference designators with W1)	14304	6918-1110
J1	Not used		
J2, J3	Connector, 26 Pin	14304	J25-0003-226
J4	Connector, 20 Pin	14304	J25-0003-220
J5	Connector, 26 Pin	14304	J25-0003-226
J6	Connector, 2 Pin	14304	J46-0012-002
S1	Switch, Rotary	14304	S65-0002-000
XA1	Connector, 40 Pin	14304	J41-0005-040
XA2	Connector, 40 Pin	14304	J25-0003-240
XA3, XA4	Connector, 40 Pin	14304	J41-0005-040
XA5	Connector, 25 Pin	14304	J41-0005-025
XPS1	Connector, 25 Pin	14304	J41-0005-025

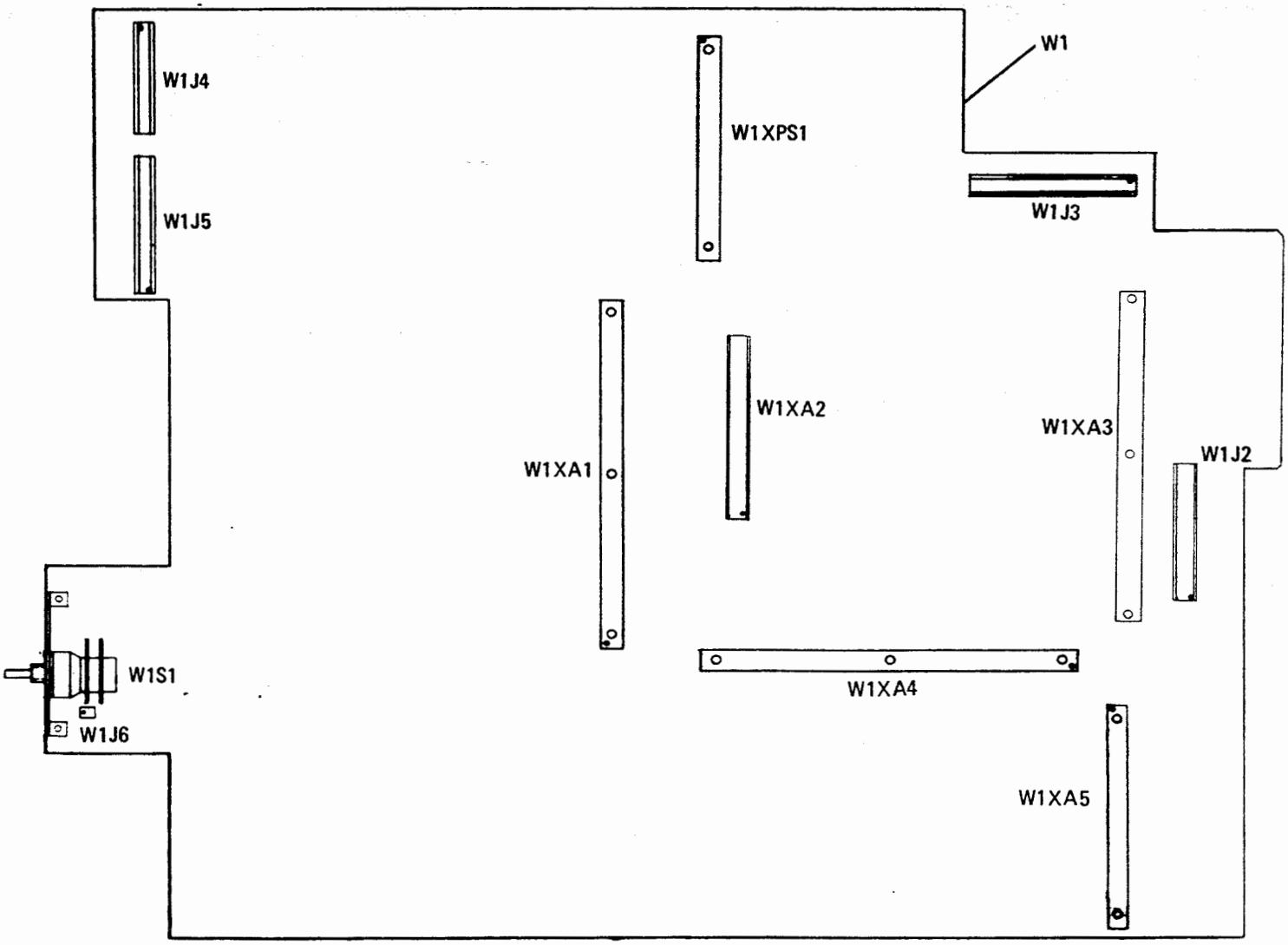


Figure 6-10. Interconnection Pwb W1 Component Locations

Table 6-11. CHASSIS AND PANEL WIRING ASSEMBLY W2 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
W2	Chassis and Panel Wiring Assembly (Note: Prefix all reference designations with W2)	14304	6918-0110
P1	Connector	14304	J42-0007-006
P2	Connector	14304	J42-0007-002

Table 6-12. RS-232 INTERFACE WIRING ASSEMBLY W3 PARTS LIST

REf. Desig.	Name and Description	Mfr.	Part No.
W3	RS-232 Interface Wiring Assembly (Note: Prefix all reference designators with W3)	14304	6918-0130
J1, J2	Not used		
J3	Connector, Female	14304	J25-0006-002
P1, P2	Not used		
P3	Connector, Socket	14304	J25-0001-003

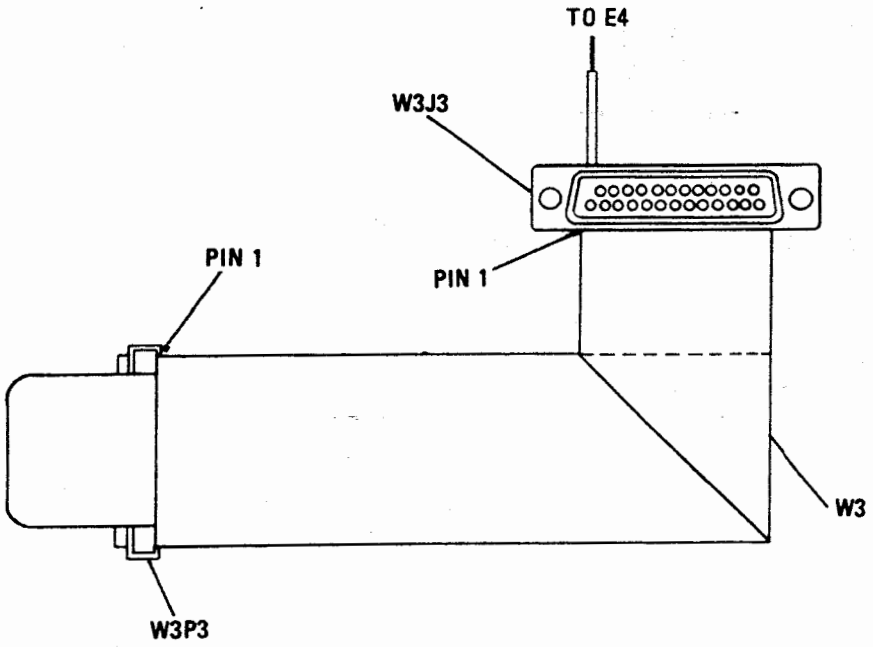


Figure 6-11. Interface Wiring Assembly W3 Component Locations

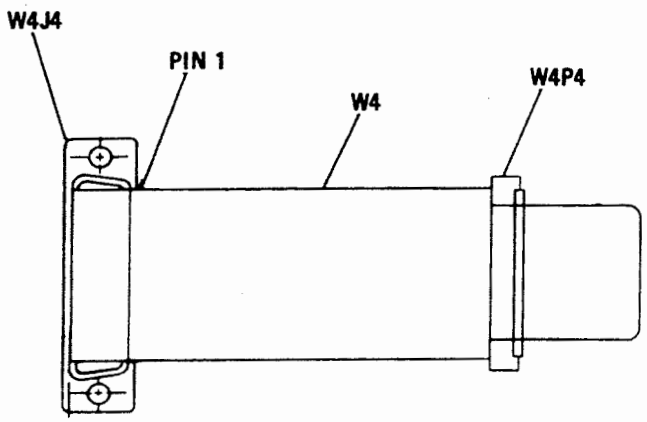


Figure 6-12. Low Level Wiring Assembly W4 Component Locations

Table 6-13. LOW LEVEL WIRING ASSEMBLY W4 PARTS LIST

Ref. Desig.	Name and Description	Mfr.	Part No.
W4	Low Level Wiring Assembly (Note: Prefix all reference designators with W4)	14304	6918-0140
J1 to J3	Not used		
J4	Connector, Male	14304	J25-0006-001
P1 to P3	Not used		
P4	Connector, Socket	14304	J25-0001-003

SECTION 7

SCHEMATIC DIAGRAMS AND RELATED DATA

7.1 INTRODUCTION

This section contains the schematic diagrams and related data necessary for circuit analysis and maintenance of the RF-3352 FSK Terminal. For complete circuit description and functional analysis, refer to Section 4 of this manual. Component location and part identification data are given in Section 6.

7.2 SCHEMATIC DIAGRAM LIST

Table 7-1 lists the figure number, title, and page number of the schematic diagrams contained in this section.

7.3 ABBREVIATIONS AND ACRONYMS

Table 7-2 lists and defines the abbreviations and acronyms used in the schematic diagrams and connector pin tables of this section.

7.4 CONNECTOR PIN, ADJUSTMENT, AND TEST POINT REFERENCE DATA

Tables 7-3 through 7-14 contain a functional description of all connector pins, adjustment potentiometers, and test points of the terminal. These tables can be used as a quick reference during troubleshooting and circuit analysis of the terminal.

Table 7-1. RF-3352 FSK TERMINAL SCHEMATIC DIAGRAM LIST

Ref. Desig.	Part Number	Schematic Diagram Figure No.	Nomenclature
--	6918-1100	7 - 1	Chassis and Panel Assembly
A1	6918-1120	7 - 2	Modulator Pwb Assembly
A2	6918-1130	7 - 3	Demodulator Pwb Assembly
A3	6918-1140	7 - 4	Timing and Control Pwb Assembly
A4	6918-1150	7 - 5	Interface Pwb Assembly
A5	6918-1190	7 - 6	Transistor/Regulator Pwb Assembly
A6	6918-1210	7 - 7	Control and Indicator Pwb Assembly
A7	6918-1220	7 - 8	Frequency Control Board Assembly
PS1	6918-1160	7 - 9	Power Supply Pwb Assembly
W1	6918-1110	7 - 10	Interconnection Pwb Assembly
W2	6918-0110	7 - 1	Chassis and Panel Wiring Assembly
W3	6918-0130	7 - 1	RS-232 Interface Wiring Assembly
W4	6918-0140	7 - 1	Low Level Wiring Assembly

Table 7-2. ABBREVIATIONS AND ACRONYMS USED IN THE SCHEMATIC DIAGRAMS

Abbreviation or Acronym	Definition
ASDL	AUTO START DRIVE LOW
C + S	CENTER PLUS SHIFT
C - S	CENTER MINUS SHIFT
CCTS	CMOS LEVEL CLEAR-TO-SEND
CDTR	CMOS LEVEL DATA TERMINAL READY
CFH1	CENTER FREQUENCY HUNDREDS 1
CFH2	CENTER FREQUENCY HUNDREDS 2
CFH4	CENTER FREQUENCY HUNDREDS 4
CFH8	CENTER FREQUENCY HUNDREDS 8
CFTH1	CENTER FREQUENCY THOUSANDS 1
CFTH2	CENTER FREQUENCY THOUSANDS 2
CFTN1	CENTER FREQUENCY TENS 1
CFTN2	CENTER FREQUENCY TENS 2
CFTN4	CENTER FREQUENCY TENS 4
CFTN8	CENTER FREQUENCY TENS 8
CFUN5	CENTER FREQUENCY UNITS 5
CRDTAL	CMOS RECEIVED DATA LOW
CRTS	CMOS LEVEL REQUEST TO SEND
CTS	CLEAR-TO-SEND
1 - (C + S)	INTERMEDIATE FREQUENCY MINUS CENTER PLUS SHIFT
1 - (C - S)	INTERMEDIATE FREQUENCY MINUS CENTER MINUS SHIFT
1LPT DR	INPUT LOOP TO PASS TRANSISTOR DRIVE
1LPT FB	INPUT LOOP TO PASS TRANSISTOR FEEDBACK
1LPT IN	INPUT LOOP TO PASS TRANSISTOR INPUT
LTCH	LATCH
MAA	MARK ANTI-ALIASING
OLPT OUT	OUTPUT LOOP TO PASS TRANSISTOR OUTPUT
OLPT FB	OUTPUT LOOP TO PASS TRANSISTOR FEEDBACK
OLPT DR	OUTPUT LOOP TO PASS TRANSISTOR DRIVE
OLPT IN	OUTPUT LOOP TO PASS TRANSISTOR INPUT
PSDTR	PSEUDO DATA TERMINAL READY
SAA	SPACE ANTI-ALIASING
SHH1	SHIFT HUNDREDS 1
SHH2	SHIFT HUNDREDS 2
SHH4	SHIFT HUNDREDS 4
SHTN1	SHIFT TENS 1
SHTN2	SHIFT TENS 2
SHTN4	SHIFT TENS 4
SHTN8	SHIFT TENS 8
SHUTL	SHIFT UNITS LEAST SIGNIFICANT
SHUTM	SHIFT UNITS MOST SIGNIFICANT
SIGDETH	SIGNAL DETECT HIGH

Table 7-3. MODULATOR PWB ASSEMBLY A1, PN 6918-1120 CONNECTOR PIN, ADJUSTMENT POT. AND TEST POINT REFERENCE DATA

CONNECTOR J1 PIN DATA

Conn.	Function	Conn.	Function
J1-1	Keyline	J1-21	Not Used
-2	+V Comm (Ground Direct to Power Supply)	-22	C - S
-3	+V (+12 Vdc Reg.(Direct to Power Supply)	-23	31 Hz CL
-4	Output Level Meter Drive	-24	LTCH
-5	CMOS Level Clear-to-Send (CCTS) ⚠1	-25	C + S
-6	Audio Output No. 2 Balanced	-26	500 Hz CL
-7	Audio Output No. 2	-27	NORM Position (to A6S2)
-8	Keyline	-28	Hand Key Input
-9	-12 Vdc	-29	Not Used
-10	Audio Output No. 1 Balanced	-30	Not Used
-11	Audio Output No. 1	-31	Not Used
-12	Audio Strap	-32	Not Used
-13	To Keyline LED	-33	Keyed
-14	Not Used	-34	CMOS Level Data Term Ready (CDTR)
-15	+12 Vdc	-35	CMOS Level Request-to-Send (CRTS)
-16	+12 Vdc	-36	OPEN Position (To A6S1)
-17	+12 Vdc	-37	OFF Position (To A6S2)
-18	Ground	-38	CLOSED Position (to A6S1)
-19	Ground	-39	Tx Data 2
-20	Ground	-40	128 Hz Input
	⚠1 High = Clear-to-Send		⚠2 1 = Mark

TEST POINT REFERENCE DATA

Test Point (A1)	Name
TP1	200X MARK TONE
TP2	200X SPACE TONE
TP3	TX DATA
TP4	CMOS SEND
TP5	200X AUDIO OUTPUT
TP6	STEP SINUSOID

ADJUSTMENT POT REFERENCE DATA

Pot (A1)	Name
R18	AUDIO OUT ADJ.
R23	AUDIO LEVEL METER CAL.
R30	TRAF. HOLD TIME
R32	CLEAR-TO-SEND DELAY

Table 7-4. DEMODULATOR PWB ASSEMBLY A2, PN 6918-1130, CONNECTOR PIN, ADJUSTMENT POT., AND TEST POINT REFERENCE DATA

CONNECTOR J1 PIN REFERENCE DATA

(Note: This connector is used in Channelized Units Only)

Conn.	Function	Conn.	Function
J1-1	Not Used	J1-14	REV. Position (to A6S3)
-2	Not Used	-15	NORM. Position (to A6S3)
-3	Not Used	-16	Not Used
-4	Not Used	-17	Ground
-5	Not Used	-18	CRDTAL
-6	250 Hz	-19	128 kHz
-7	I - (C + S)	-20	7.8125 Hz
-8	31 Hz CL	-21	Not Used
-9	LTCH	-22	Not Used
-10	I - (C - S)	-23	Not Used
-11	62.5 Hz	-24	Not Used
-12	SIGDETH	-25	Not Used
-13	+ 12 Vdc	-25	Not Used

CONNECTOR J2 PIN REFERENCE DATA

(Note: This connector is used in Channelized Units Only)

Conn.	Function	Conn.	Function
J2-1	Not Used	J2-14	Ref. Lvl. Meter Drive -
-2	Not Used	-15	8 kHz
-3	Not Used	-16	16 kHz
-4	Not Used	-17	32 kHz
-5	Not Used	-18	Audio Input - Balanced
-6	AGC Level -	-19	Audio Input
-7	Ground	-20	Meter Drive +
-8	Ref. Lvl. Meter Drive +	-21	-12 Vdc
-9	-12 Vdc	-22	Diversity Connection (Gain)
-10	ASDL	-23	Not Used
-11	+ 12 Vdc	-24	Not Used
-12	Diversity Connection (Signal)	-25	Not Used
-13	AGC Level +		

Table 7-4. DEMODULATOR PWB ASSEMBLY A2, PN 6918-1130 CONNECTOR PIN, ADJUSTMENT POT., AND TEST POINT REFERENCE DATA (Cont.)

CONNECTOR J3 PIN REFERENCE DATA

Conn.	Function	Conn.	Function
J3-1	REV. Position (to A6S3)	J3-11	31 Hz CL
-2	+ 12 Vdc	-12	I - (C + S)
-3	SIGDETH	-13	7.8125 Hz
-4	62.5 Hz	-14	128 Hz
-5	Not Used	-15	250 Hz
-6	NORM, Position (to A6S3)	-16	Not Used
-7	I - (C - S)	-17	Not Used
-8	LTCH	-18	Not Used
-9	CRDTAL	-19	Not Used
-10	Ground	-20	Not Used

CONNECTOR J4 PIN REFERENCE DATA

Conn.	Function	Conn.	Function
J4-1	-12 Vdc	J4-11	Diversity Connection (Gain)
-2	Ref. Lvl. Meter Drive + (to W1S1A-1)	-12	Not Used
-3	+ 12 Vdc	-13	8 kHz
-4	Ground	-14	AGC Level +
-5	ASDL	-15	Meter Drive +
-6	Not Used	-16	-12 Vdc
-7	AGC Level	-17	32 kHz
-8	Not Used	-18	16 kHz
-9	Ref. Lvl. Meter Drive -	-19	Audio Input$_{Balanced}$
-10	Diversity Connection (Signal)	-20	Audio Input

CONNECTOR P1 PIN REFERENCE DATA

Conn.	Function	Conn.	Function	Conn.	Function
P1-1	REV. Position (to A6S3)	P1-15	250 Hz		
-2	+ 12 Vdc	-16	Not Used		
-3	SIGDETH	-17	Not Used	P1-29	Ref. Lvl. Meter Drive -
-4	62.5 Hz	-18	Not Used	-30	Diversity Conn. (Signal)
-5	Not Used	-19	Not Used	-31	Diversity Conn. (Gain)
-6	NORM Position (to A6S3)	-20	Not Used	-32	Not Used
-7	I - (C - S)	-21	-12 Vdc	-33	8 kHz
-8	LTCH	-22	Ref. Lvl. Meter Drive + (to W1S1A-1)	-34	AGC Level +
-9	CRDTAL	-23	+ 12 Vdc	-35	Meter Drive +
-10	Ground	-24	Ground	-36	-12 Vdc
-11	31 Hz CL	-25	ASDL	-37	32 kHz
-12	I - (C + S)	-26	Not Used	-38	16 kHz
-13	7.8125 Hz	-27	AGC Level	-39	Audio Input$_{Balanced}$
-14	128 Hz	-28	Not Used	-40	Audio Input

Table 7-4. DEMODULATOR PWB ASSEMBLY A2, PN 6918-1130 CONNECTOR PIN, ADJUSTMENT POT., AND TEST POINT REFERENCE DATA (Cont.)

TEST POINT REFERENCE DATA

Test Point (A2)	Name	Test Point (A2)	Name
TP1	MARK L.O. FREQUENCY	TP10	SPACE ENVELOPE
TP2	SPACE L.O. FREQUENCY	TP11	MAA
TP3	SLICER OUTPUT	TP12	MARK BPF OUT
TP4	VALID DATA DET. (1)	TP13	MARK ENVELOPE
TP5	CMOS RCV DATA (2)	TP14	DECISION LEVEL
TP6	MARK MIX. OUT	TP15	COMPOSITE ENVELOPE
TP7	SPACE MIX. OUT	TP16	GAIN CONT. V.
TP8	SAA	TP17	CHASSIS GROUND
TP9	SPACE BPF OUT	TP18	CHASSIS GROUND

(1) 1 = Signal (2) Low = Mark

ADJUSTMENT POT. REFERENCE DATA

Pot (A2)	Name
R19	MARK MIX. BAL.
R31	AUDIO BAL.
R50	SPACE MIX. BAL.
R52	SAA TUNE
R59	SPACE BPF Trim.
R74	MAA TUNE
R81	MARK BPF TRIM.
R131	AGC BIAS ADJUST
R136	AGC GAIN ADJUST
R166	AUDIO IN METER ADJUST

Table 7-5. TIMING AND CONTROL PWB ASSEMBLY A3, PN 6918-1140 CONNECTOR PIN AND TEST POINT REFERENCE DATA

CONNECTOR J1 PIN REFERENCE DATA

Conn.	Function	Conn.	Function
J1-1	CFUN5	J1-21	Common
-2	CFTH2	-22	+ 12 Vdc
-3	CFTH1	-23	C + S
-4	CFH1	-24	SHUTM
-5	CFH2	-25	SHUTL
-6	CFH4	-26	I - (C + S)
-7	CFH8	-27	C - S
-8	CFTN2	-28	I - (C - S)
-9	CFTN4	-29	Not Used
-10	CFTN1	-30	7.8125HZ
-11	CFTN8	-31	500 HZ Clock
-12	SHTN1	-32	250 HZ Clock
-13	SHH4	-33	62.5 HZ
-14	SHH1	-34	64 KHZ
-15	SHTN8	-35	128KHZ
-16	SHTN4	-36	32 KHZ
-17	SHTN1	-37	16 KHZ
-18	SHTN2	-38	8 KHZ
-19	+ 12 Vdc	-39	31 HZ Clock
-20	Common	-40	Latch

TEST POINT REFERENCE DATA

Test Point (A3)	Name
TP1	OSC OUT
TP2	8 KHZ
TP3	C + S
TP4	I - (¼c + S)
TP5	C - S
TP6	I - (C - S)

Table 7-6. INTERFACE PWB ASSEMBLY A4, PN6918-1150 CONNECTOR PIN, ADJUSTMENT POT., AND SWITCH REFERENCE DATA

NOTE: There are no test points on this assembly.

CONNECTOR J1 PIN REFERENCE DATA

Conn.	Function	Conn.	Function
J1-1	Data Input	J1-21	Transmitted
-2	Meter-Input	-22	TTY Drive
-3	ILPT Out	-23	+ 65 Vdc Input
-4	Meter + Input	-24	-65 Vdc Input
-5	ILPT FB	-25	Not Used
-6	ILPT DR	-26	-12 Vdc Input
-7	ILPT In	-27	Common
-8	Data Input	-28	+ 12 Vdc Input
-9	Data Set Ready	-29	Not Used
-10	CTS	-30	Meter Out -
-11	CCTS (1)	-31	OLPT Out
-12	SIGDETH (2)	-32	OLPT In
-13	CRDTAL (3)	-33	Meter Out +
-14	Received Data	-34	OLPT FB
-15	Rcvd. In. Sig. Det.	-35	OLPT DR
-16	Mod Data (4)	-36	Not Used
-17	CDTR	-37	-12 Vdc (Unreg.)
-18	CRTS	-38	Relay Drive
-19	Request to Send	-39	Ground (separate run back to Pwr
-20	Data Terminal Ready	-40	ASDL Sply)

(1) HIGH = Clear-to-Send (2) HIGH = Signal (3) LOW = MARK 4 1 = MARK

SWITCH REFERENCE DATA

Switch (A4)	Name
S1	NEUTRAL-POLAR
S2	PSDTR
S3	AS OVERRIDE

ADJUSTMENT POT. REFERENCE DATA

Pot. (A4)	Name
R1	INPUT LOOP METER CAL. ADJ.
R25	OUTPUT LOOP METER CAL. ADJ.

Table 7-7. TRANSISTOR REGULATOR PWB ASSEMBLY A5, PN 6918-1190 CONNECTOR PIN, ADJUSTMENT., AND SWITCH REFERENCE DATA

NOTE: There are no test points on this assembly.

CONNECTOR J1 AND J2 PIN REFERENCE DATA

CONN.	FUNCTION	CONN.	FUNCTION
J1-1	Audio Input	J1-14	+ 12 Vdc (Reg.)
-2	Audio Input	-15	ILPT DR
-3	Audio Input	-16	ILPT In
-4	Audio Input	-17	ILPT FB
-5	Audio Out (1)	-18	ILPT Out
-6	Audio Out (1)	-19	OLPT FB
-7	Audio Out (1)	-20	OLPT Out
-8	Audio Out (1)	-21	OLPT In
-9	Relay Drive	-22	OLPT DR
-10	-12 Vdc (Unreg.)	-23	Not Used
-11	-12 Vdc (Reg.)	-24	Not Used
-12	+ 12 Vdc (Unreg.)	-25	Not Used
-13	Ground	J2-1	-12 Vdc (Unreg.)
		J2-2	Relay Drive

ADJUSTMENT POT. REFERENCE DATA

Pot. (A5)	Name
R1	OUTPUT LOOP ADJUST
R2	INPUT LOOP ADJUST

SWITCH REFERENCE DATA

Switch (A5)	Name
S1	NORM ◄► LOOP BACK

Table 7-8. CONTROL AND INDICATOR PWB ASSEMBLY A6 PN 6918-1210 CONNECTOR PIN, LED, AND SWITCH REFERENCE DATA

NOTE: There are no test points on this assembly.

CONNECTOR J1 AND P1 PIN REFERENCE DATA

Conn.	Function	Conn.	Function
J1/P1-1	CLOSED Terminal (A6S1-3)	J1/P1-11	Not Used
2	Ground	-12	NORM Terminal (A6S2-1)
-3	CLOSED (LEDA6DS1 Anode)	-13	Not Used
-4	OPEN Terminal (A6S1-1)	-14	Not Used
-5	Not Used	-15	Not Used
-6	Not Used	-16	OFF Terminal (A6S2-3)
-7	Not Used	-17	SIGDETH (1)
-8	+ 12 Vdc	-18	CRDTAL (2)
-9	Not Used	-19	NORM Terminal (A6S31)
-10	Not Used	-20	REV Terminal (A6S3-3)

(1) 1 = Signal (2) Low = Mark

LED INDICATOR REFERENCE DATA

Ref. Desig. (A6)	Name and Function
DS1	Transmit - CLOSED Indicator
DS2	Receive Status - SPACE Indicator
DS3	Receive Status - MARK Indicator
DS4	Receive Status - SIGNAL Indicator

SWITCH REFERENCE DATA

Ref. Desig. (A6)	Name and Function
S1	Transmit OPEN-AUTO-CLOSED Switch
S2	Transmit NORM-REV-OFF Switch
S3	Receive NORM-MARK HOLD-REV Switch

Table 7-9. FREQUENCY CONTROL BOARD ASSEMBLY A7, PN 6918-1220 CONNECTOR PIN AND SWITCH REFERENCE DATA

NOTE: There are no test points or adjustments on this assembly.

CONNECTOR J1 PIN REFERENCE DATA

Conn.	Function	Conn.	Function
J1-1	CFTN4	J1-14	Ground
-2	CFH2	-15	Ground
-3	CFH1	-16	SHH4
-4	CFH4	-17	SHH1
-5	CFTN2	-18	Not Used
-6	CFTN8	-19	SHH2
-7	CFH8	-20	SHTN2
-8	CFTH2	-21	Not Used
-9	CFUN5	-22	SHUTM
-10	CFTN1	-23	SHTN1
-11	CFTH1	-24	SHTN4
-12	Ground	-25	SHTN8
-13	Ground	-26	SHUTL

CONNECTOR P1 PIN REFERENCE DATA

Conn.	Function	Conn.	Function
P1-1	CFTN4	P1-14	CFH2
-2	CFH1	-15	CFH4
-3	CFTN2	-16	CFTN8
-4	CFH8	-17	CFTH2
-5	CFUN5	-18	CFTN1
-6	CFTH1	-19	Ground
-7	Ground	-20	Ground
-8	Ground	-21	SHH4
-9	SHH1	-22	Not Used
-10	SHH2	-23	SHTN2
-11	Not Used	-24	SHUTM
-12	SHTN1	-25	SHTN4
-13	SHTN8	-26	SHUTL

SWITCH A7S1 REFERENCE DATA

Reference Designator (A7)	Name or Function
S1A through S1D	CENTER FREQUENCY Switches
S1E through S1G	SHIFT Frequency Switches

Table 7-10. POWER SUPPLY PWB ASSEMBLY PS1, PN 6918-1160 CONNECTOR PIN AND FUSE REFERENCE DATA

CONNECTOR J1 PIN REFERENCE DATA

Conn.	Function	Conn.	Function
J1-1	Not Used	J1-13	Not Used
-2	Not Used	-14	Not Used
-3	+ 12 Vdc (Unreg.)	-15	Not Used
-4	-12 Vdc (Unreg.)	-16	Not Used
-5	Not Used	-17	Loop Common
-6	-65 Vdc	-18	Loop Common
-7	-65 Vdc	-19	Not Used
-8	Not Used	-20	Ground
-9	Not Used	-21	Ground
-10	Not Used	-22	Not Used
-11	Not Used	-23	+ 65 Vdc
-12	Not Used	-24	+ 65 Vdc

CONNECTOR J2 PIN REFERENCE DATA

Conn.	Function
J2-1	-19.5 Vrms
-2	Ground
-3	+ 19.5 Vrms
-4	+ 62.5 Vrms
-5	Common
-6	-62.5 Vrms

FUSE DATA

Ref. Desig.	Rating
F1	1/8 Ampere, 250V
F2	1/8 Ampere, 250V

Table 7-11. INTERCONNECTION PWB ASSEMBLY W1, PN 6918-1110 CONNECTOR PIN REFERENCE DATA

CONNECTOR J1 PIN REFERENCE DATA (MATES WITH CHASSIS CONNECTOR J5)

Conn.	Function	Conn.	Function
J1-1	Not Used	J1-6	Loop Supply - Comm.
-2	Data In	-7	Loop Supply - Pos.
-3	Data In	-8	+60 Vdc In
-4	-60 Vdc In	-9	Data Out
-5	Loop Supply - Neg.	-10	Not Used

CONNECTOR J2PIN REFERENCE DATA (MATES WITH LOW LEVEL WIRING ASSEMBLY W4 CONNECTOR W4P4)

Conn.	Function	Conn.	Function
J2-1	Audio Input	J2-14	Audio In
-2	Audio Output No. 1	-15	Ground
-3	Ground	-16	Audio Output No. 1
-4	Audio Output No. 2	-17	Audio Output No. 2
-5	Ground	-18	Ground
-6	Div. Signal	-19	Div. Signal
-7	Div. Gain	-20	Div. Gain
-8	Keyline	-21	Ground
-9	Ground	-22	Keyline
-10	Not Used	-23	Hand Key Input
-11	Ground	-24	Ground
-12	Audio Strap	-25	Audio Strap
-13	Not Used	-26	Not Used

CONNECTOR J3 PIN REFERENCE DATA (MATES WITH RS-232 INTERFACE WIRING ASSEMBLY W3 CONNECTOR W3J3)

Conn.	Function	Conn.	Function
J3-1	Protective Ground	J3-14	Not Used
-2	Trans. Data	-15	Not Used
-3	Rec. Data	-16	Not Used
-4	Req.-to-Send	-17	Not Used
-5	Clear-to-Send	-18	Not Used
-6	Data Set Ready	-19	Not Used
-7	System Ground	-20	Data Term. Ready
-8	Rcvd. In. Sig. Det.	-21	Not Used
-9	Not Used	-22	Not Used
-10	Not Used	-23	Not Used
-11	Not Used	-24	Not Used
-12	Not Used	-25	Not Used
-13	Not Used	-26	Not Used

Table 7-11. INTERCONNECTION PWB ASSEMBLY W1, PN 6918-1110 CONNECTOR PIN REFERENCE DATA (Cont.)

CONNECTOR J4 PIN REFERENCE DATA (MATES WITH CONTROL AND INDICATOR PWB A6 CONNECTOR A6P1)

Conn.	Function	Conn.	Function
J4-1	CLOSED Position (to A6S1)	J4-11	Not Used
-2	Ground	-12	NORM Position (to A6S2)
-3	CLOSED LED (to A6DS1)	-13	Not Used
-4	OPEN Position	-14	Not Used
-5	Not Used	-15	Not Used
-6	Not Used	-16	OFF Position (to A6S2)
-7	Not Used	-17	SIGDETH 1
-8	+ 12 Vdc	-18	CRDTAL 2
-9	Not Used	-19	NORM Position (to A6S3)
-10	Not Used	-20	REV Position (to A6S3)

1 1 = Signal 2 Low = Mark

CONNECTOR J5 PIN REFERENCE DATA (MATES WITH FREQUENCY CONTROL BOARD ASSEMBLY A7 CONNECTOR A7P1)

Conn.	Function	Conn.	Function
J5-1	CFTN4	J5-14	CFH2
-2	CFH1	-15	CFH4
-3	CFTN2	-16	CFTN8
-4	CFH8	-17	CFTH2
-5	CFUN5	-18	CFTN1
-6	CFTH1	-19	Ground
-7	Ground	-20	Ground
-8	Ground	-21	SHH4
-9	SHH1	-22	Not Used
-10	SHH2	-23	SHTN2
-11	Not Used	-24	SHUTM
-12	SHTN1	-25	SHTN4
-13	SHTN8	-26	SHUTL

CONNECTOR J6 PIN REFERENCE DATA (MATES WITH CHASSIS AND PANEL WIRING ASSEMBLY W2 CONNECTOR W2P2)

Conn.	Function	Conn.	Function
J6-1	Meter Drive (+)	J6-2	Meter Return (-)

Table 7-11. INTERCONNECTION PWB ASSEMBLY W1, PN 6918-1110 CONNECTOR PIN REFERENCE DATA (Cont.)

CONNECTOR XA1 PIN REFERENCE DATA (MATES WITH MODULATOR PWB ASSEMBLY A1 CONNECTOR A1J1)

Conn.	Function	Conn.	Function
XA1-1	Keyline	XA1-21	Not Used
-2	+V Comm (Ground Direct to Power Supply)	-22	C - S
		-23	31 Hz CL
-3	+V (+12 Vdc [Reg] Direct to Power Supply)	-24	LTCH
		-25	C + S
-4	Output Level Meter Drive	-26	500 Hz CL
-5	CCTS	-27	NORM Position (to A6S2)
-6	Audio Output No. 2	-28	Hand Key Input
-7	Audio Output No. 2	-29	Not Used
-8	Keyline	-30	Not Used
-9	-12 Vdc	-31	Not Used
-10	Audio Output No. 1	-32	Not Used
-11	Audio Output No. 1	-33	Not Used
-12	Audio Strap	-34	CDTR
-13	To Keyline LED	-35	CRTS
-14	Not Used	-36	OPEN Position (to A6S1)
-15	+12 Vdc	-37	OFF Position (to A6S2)
-16	+12 Vdc	-38	CLOSED Position (to A6S1)
-17	+12 Vdc	-39	TX Data
-18	Ground	-40	128 KHZ Input
-19	Ground		
-20	Ground		

Table 7-11. INTERCONNECTION PWB ASSEMBLY W1, PN 6918-1110 CONNECTOR PIN REFERENCE DATA (Cont.)

CONNECTOR XA2 PIN REFERENCE DATA (MATES WITH DEMODULATOR PWB ASSEMBLY A2, CONNECTOR A2P1)

Conn.	Function	Conn.	Function
XA2-1	REV. Position (to A6S3)	XA2-21	-12 Vdc
-2	+ 12 Vdc	-22	Ref. Lvl. + (to W1S1A-1)
-3	SIGDETH	-23	+ 12 Vdc
-4	62.5 Hz	-24	Ground
-5	Not Used	-25	ASDL
-6	NORM Position (to A6S3)	-26	Not Used
-7	I - (C - S)	-27	AGC Level - (to W1S1B-12)
-8	LTCH	-28	Not Used
-9	CRDTAL	-29	Ref. Lvl. - (to W1S1B-1)
-10	Ground	-30	Div. Sig.
-11	31 Hz CL	-31	Div. Gain
-12	I - (C + S)	-32	Not Used
-13	7.8125 Hz	-33	8 KHz
-14	128 KHz	-34	AGC Level + (to W1S1A-12)
-15	250 Hz	-35	Input Lvl. + (to W1S1A-2)
-16	Not Used	-36	-12 Vdc
-17	Not Used	-37	32 KHz
-18	Not Used	-38	16 KHz
-19	Not Used	-39	Audio Input
-20	Not Used	-40	Audio Input

Table 7-11. INTERCONNECTION PWB ASSEMBLY W1, PN 6918-1110 CONNECTOR PIN REFERENCE DATA (Cont.)

CONNECTOR XA3 PIN REFERENCE DATA (MATES WITH TIMING AND CONTROL PWB ASSEMBLY A3 CONNECTOR A3J1)

Conn.	Function	Conn.	Function
XA3-1	CFUN5	XA3-21	Common
-2	CFTH2	-22	+ 12 Vdc
-3	CFTH1	-23	(C + S)
-4	CFH1	-24	SHUTM
-5	CFH2	-25	SHUTL
-6	CFH4	-26	I - (C + S)
-7	CFH8	-27	C - D
-8	CFTN2	-28	I - (C - S)
-9	CFTN4	-29	Not Used
-10	CFTN1	-30	7.8125 Hz
-11	CFTN8	-31	500 Hz Clock
-12	SHH2	-32	250 Hz Clock
-13	SHH4	-33	62.5 Hz
-14	SHH1	-34	Not Used
-15	SHTN8	-35	128 KHz
-16	SHTN4	-36	32 KHz
-17	SHTN1	-37	16 KHz
-18	SHTN2	-38	8 KHz
-19	+ 12 Vdc	-39	31 Hz Clock
-20	Common	-40	Latch

Table 7-11. INTERCONNECTION PWB ASSEMBLY W1, PN 6918-1110, CONNECTOR PIN REFERENCE DATA (Cont.)

CONNECTOR XA4 PIN REFERENCE DATA (MATES WITH INTERFACE PWB ASSEMBLY A4 CONNECTOR A4J1)

Conn.	Function	Conn.	Function
XA4-1	Data Input	XA4-21	Transmitted Data
-2	Meter - Input	-22	TTY Drive
-3	ILPT Out	-23	+65 Vdc In
-4	Meter + In	-24	-65 Vdc In
-5	ILPT FB	-25	Not Used
-6	ILPT DR	-26	-12 Vdc Input
-7	ILPT In	-27	Ground
-8	Data Input	-28	+12 Vdc Input
-9	Data Set Ready	-29	Not Used
-10	CTS	-30	Meter Out
-11	CCTS	-31	OLPT Out
-12	SIGDETH	-32	OLPT in
-13	CRDTAL	-33	Meter Out +
-14	Received Data	-34	OLPT FB
-15	SIGDETH	-35	OLPT DR
-16	Mod. Data	-36	Not Used
-17	CDTR	-37	-12 Vdc (Unreg.)
-18	CRTS	-38	Relay Drive
-19	Request-to-Send	-39	Ground (Separate Run Back to Pwr.
-20	Data Terminal Ready	-40	ASDL Suply.)

CONNECTOR XA5 PIN REFERENCE DATA (MATES WITH TRANSISTOR/REGULATOR PWB ASSEMBLY A5 CONNECTOR A5J1)

Conn.	Function	Conn.	Function
XA5-1	Audio Input	XA5-14	+12 Vdc (Reg.)
-2	Audio Input	-15	ILPT Dr
-3	Audio Input	-16	ILPT In
-4	Audio Input	-17	ILPT FB
-5	Audio Out (1)	-18	ILPT Out
-6	Audio Out (1)	-19	OLPT FB
-7	Audio Out (1)	-20	OLPT Out
-8	Audio Out (1)	-21	OLPT In
-9	Relay Drive	-22	OLPT DR
-10	-12 Vdc (Unreg.)	-23	Not Used
-11	-12 Vdc (Reg.)	-24	Not Used
-12	+12 Vdc (Unreg.)	-25	Not Used
-13	Ground		

Table 7-11. INTERCONNECTION PWB ASSEMBLY W1, PN 6918-1110 CONNECTOR PIN REFERENCE DATA (Cont.)

CONNECTOR XPS1 PIN REFERENCE DATA (MATES WITH POWER SUPPLY PWB ASSEMBLY PS1 CONNECTOR PS1J1)

Conn.	Function	Conn.	Function
XPS1-1	Not Used	XPS1-14	Not Used
-2	Not Used	-15	Not Used
-3	+ 12 Vdc (Unreg.)	-16	Not Used
-4	-12 Vdc (Unreg.)	-17	Loop Common
-5	Not Used	-18	Loop Common
-6	-65 Vdc	-19	Not Used
-7	-65 Vdc	-20	Ground
-8	Not Used	-21	Ground
-9	Not Used	-22	Not Used
-10	Not Used	-23	+ 65 Vdc
-11	Not Used	-24	+ 65 Vdc
-12	Not Used	-25	Not Used
-13	Not Used		

Table 7-12. CHASSIS AND PANEL WIRING ASSEMBLY W2, PN 6918-0110

CONNECTOR P1 PIN REFERENCE DATA
(MATES WITH POWER SUPPLY PWB ASSEMBLY PS1 CONNECTOR PS1J2)

Conn.	Function	Conn.	Function
P1-1	T1 AC Secondary (-19.5 Vrms)	P1-4	T1 AC Secondary (+ 62.5 Vrms)
-2	T1AC Secondary Ground	-5	T1AC Secondary (Common)
-3	T1 AC Secondary (+ 19.5 Vrms)	-6	T1 AC Secondary (-62.5 Vrms)

CONNECTOR P2 PIN REFERENCE DATA
(MATES WITH INTERCONNECTION PWB ASSEMBLY W1 CONNECTOR W1J6)

Conn.	Function	Conn.	Function
P2-1	Meter Drive (+)	P2-2	Meter Return (-)

CONNECTOR P5 PIN REFERENCE DATA
(MATES WITH TRANSISTOR/REGULATOR PWB A5 CONNECTOR A5J2)

Conn.	Function	Conn.	Function
P5-1	-12 Vdc (Unreg.)	P5-2	Relay Drive

Table 7-13. RF-232 INTERFACE WIRING ASSEMBLY W3, PN 6918-0130 CONNECTOR PIN REFERENCE DATA

CONNECTOR J3 PIN REFERENCE DATA (ATTACHED TO CHASSIS REAR PANEL)

Conn.	Function	Conn.	Function
J3-1	Protective Ground	J3-14	Not Used
-2	Trans. Data	-15	Not Used
-3	Rec. Data	-16	Not Used
-4	Req.-to-Send	-17	Not Used
-5	Clear-to-Send	-18	Not Used
-6	Data Set Ready	-19	Not Used
-7	System Ground	-20	Data Term. Ready
-8	Rcvd. In. Sig. Det.	-21	Not Used
-9	Not Used	-22	Not Used
-10	Not Used	-23	Not Used
-11	Not Used	-24	Not Used
-12	Not Used	-25	Not Used
-13	Not Used		

CONNECTOR P3 PIN REFERENCE DATA (MATES WITH INTERCONNECTION PWB ASSEMBLY W1 CONNECTOR W1J3)

Conn.	Function	Conn.	Function
P3-1	Protective Ground	P3-14	Not Used
-2	Trans. Data	-15	Not Used
-3	Rec. Data	-16	Not Used
-4	Req.-to-Send	-17	Not Used
-5	Clear-to-Send	-18	Not Used
-6	Data Set Ready	-19	Not Used
-7	System Ground	-20	Data Term. Ready
-8	Rcvd. In. Sig. Det.	-21	Not Used
-9	Not Used	-22	Not Used
-10	Not Used	-23	Not Used
-11	Not Used	-24	Not Used
-12	Not Used	-25	Not Used
-13	Not Used	-26	Not Used

Table 7-14. LOW LEVEL WIRING ASSEMBLY W4, PN 6918-0140, CONNECTOR PIN REFERENCE DATA

CONNECTOR J4, PIN REFERENCE DATA (ATTACHED TO CHASSIS REAR PANEL(

Conn.	Function	Conn.	Function
J4-1	Audio Input	J4-14	Audio Input
-2	Audio Output No. 1	-15	Ground
-3	Ground	-16	Audio Output No. 1
-4	Audio Output No. 2	-17	Audio Output No. 2
-5	Ground	-18	Ground
-6	Div. Signal	-19	Div. Signal
-7	Div. Gain	-20	Div. Gain
-8	Keyline	-21	Ground
-9	Ground	-22	Keyline
-10	Not Used	-23	Hand Key Input
-11	Ground	-24	Ground
-12	Audio Strap	-25	Audio Strap
-13	Not Used		

CONNECTOR P4, PIN REFERENCE DATA (MATES WITH INTERCONNECTION PWB ASSEMBLY W1 CONNECTOR W1J2)

Conn.	Function	Conn.	Function
P4-1	Audio Input	P4-14	Audio Input
-2	Audio Output No. 1	-15	Ground
-3	Ground	-16	Audio Output No. 1
-4	Audio Output No. 2	-17	Audio Output No. 2
-5	Ground	-18	Ground
-6	Div. Signal	-19	Div. Signal
-7	Div. Gain	-20	Div. Gain
-8	Keyline	-21	Ground
-9	Ground	-22	Keyline
-10	Not Used	-23	Hand Key Input
-11	Ground	-24	Ground
-12	Audio Strap	-25	Audio Strap
-13	Not Used	-26	Not Used

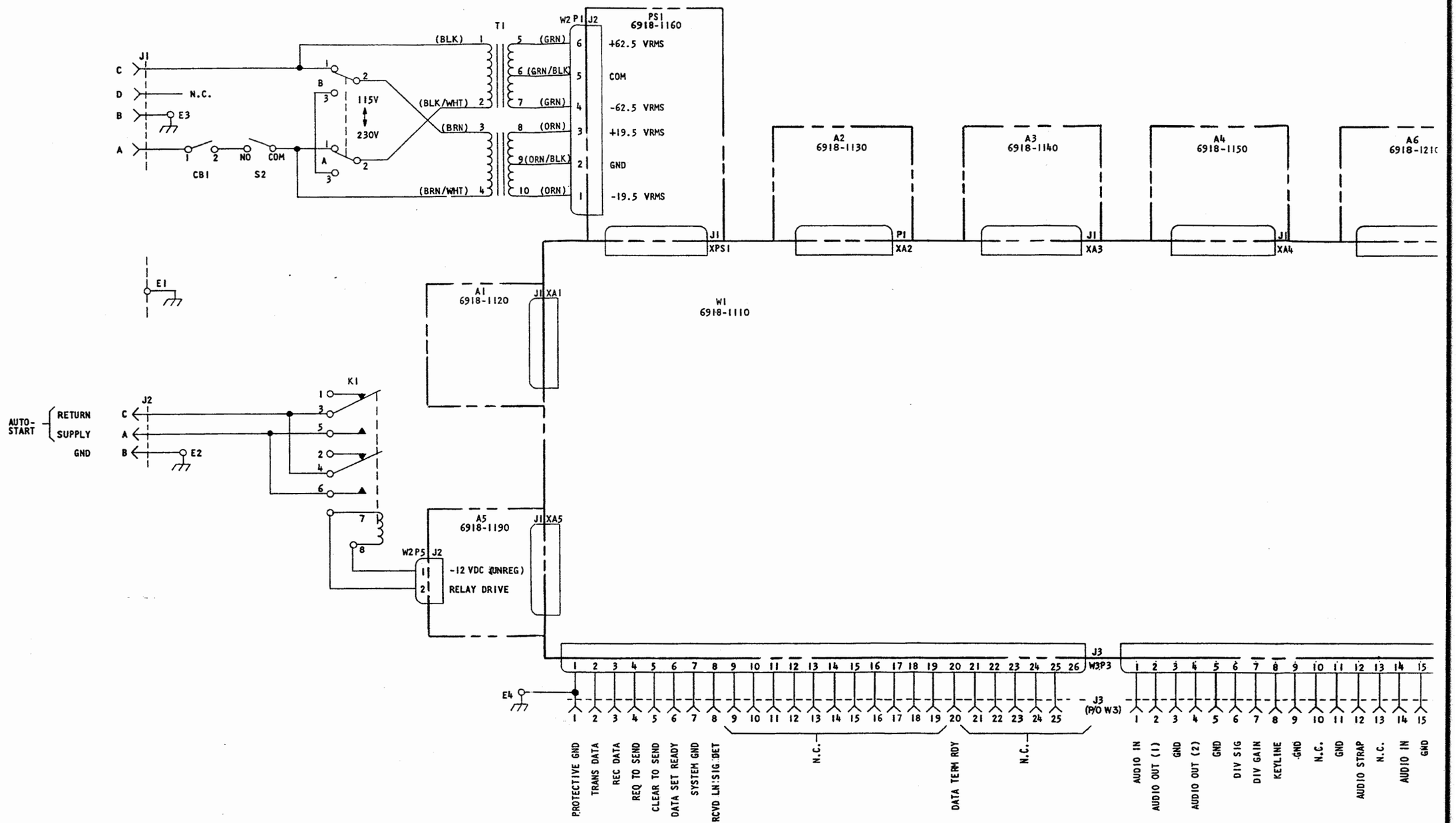


Figure 7-1. RF-33

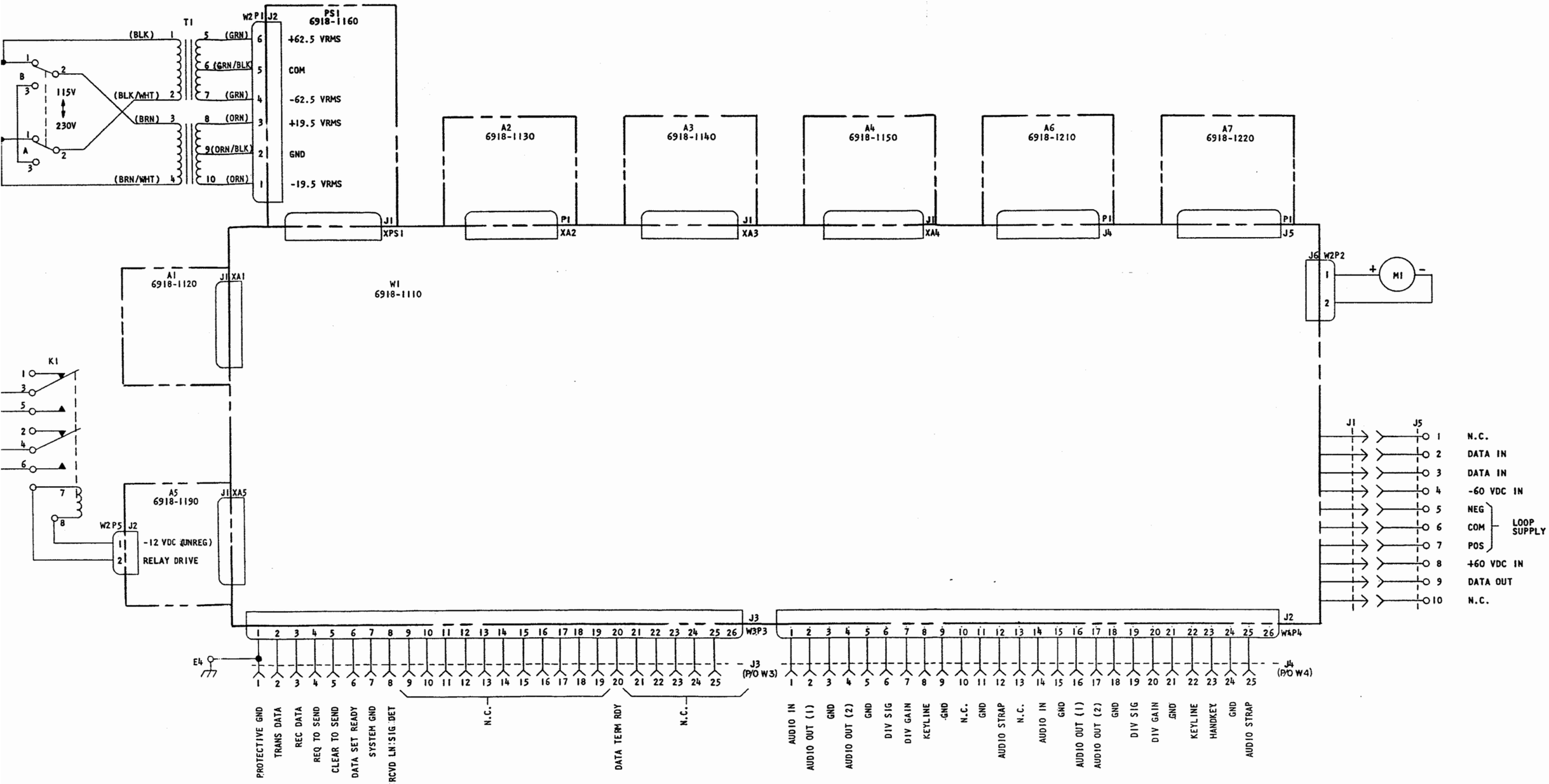
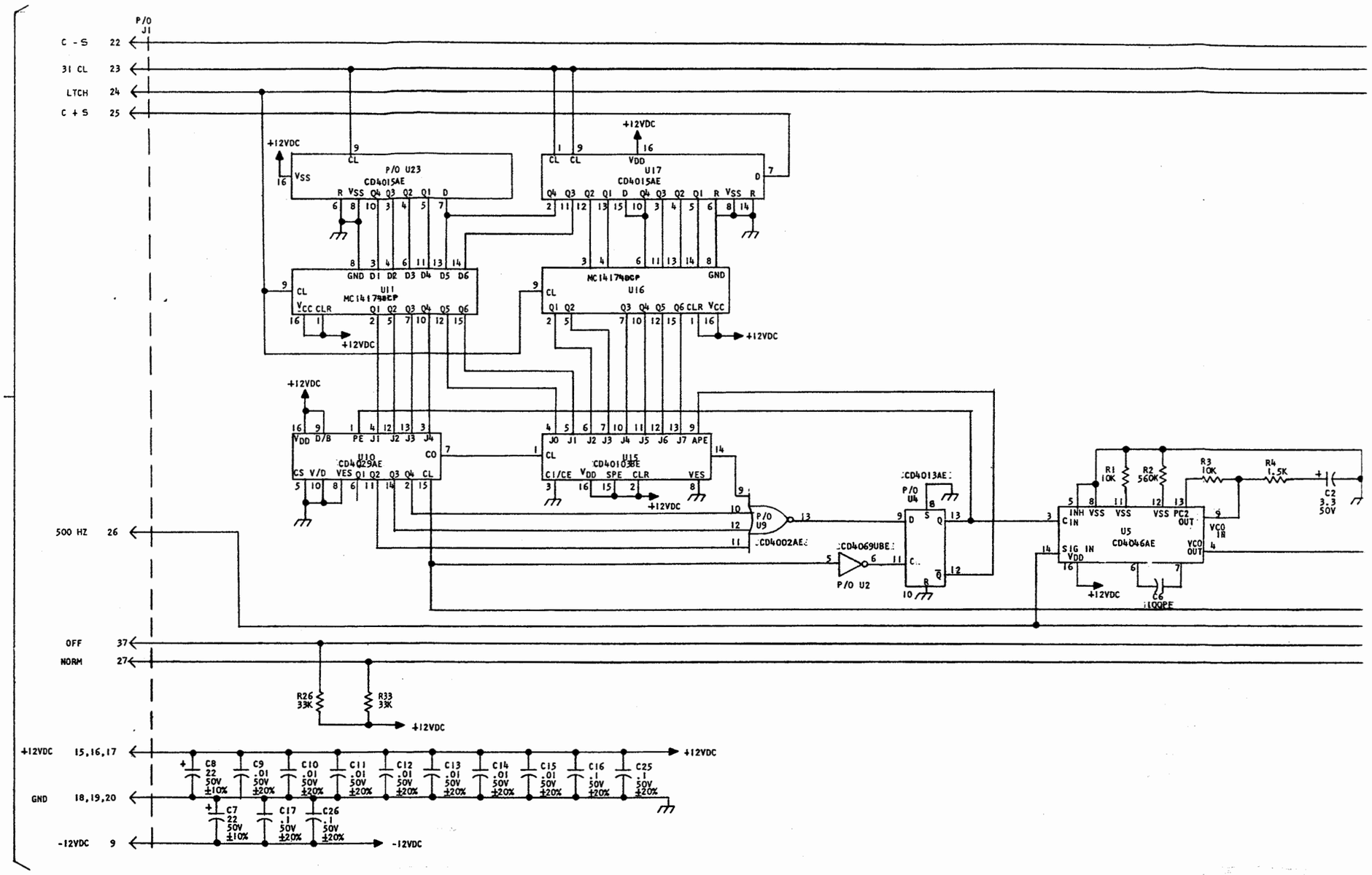


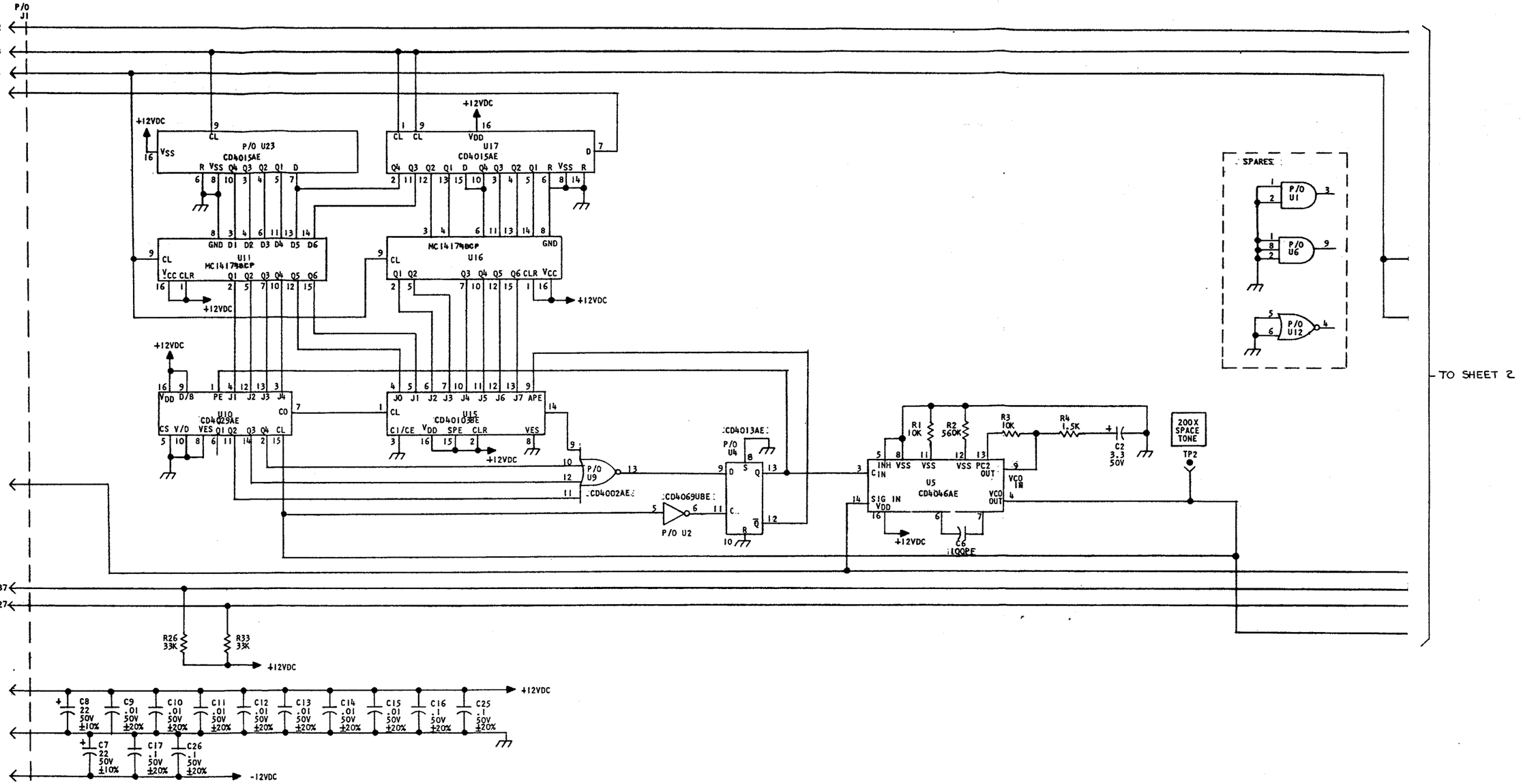
Figure 7-1. RF-3352 FSK Terminal Chassis and Panel Assembly Schematic Diagram



NOTES:

1. PREFIX ALL PARTIAL REFERENCE DESIGNATORS WITH A1.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
   ALL CAPACITORS ARE IN MICROFARADS.

Figure 7-2.



NOTES:

1. PREFIX ALL PARTIAL REFERENCE DESIGNATORS WITH A1.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
   ALL CAPACITORS ARE IN MICROFARADS.

Figure 7-2. Modulator Pwb A1 Schematic Diagram (Sheet 1 of 4)

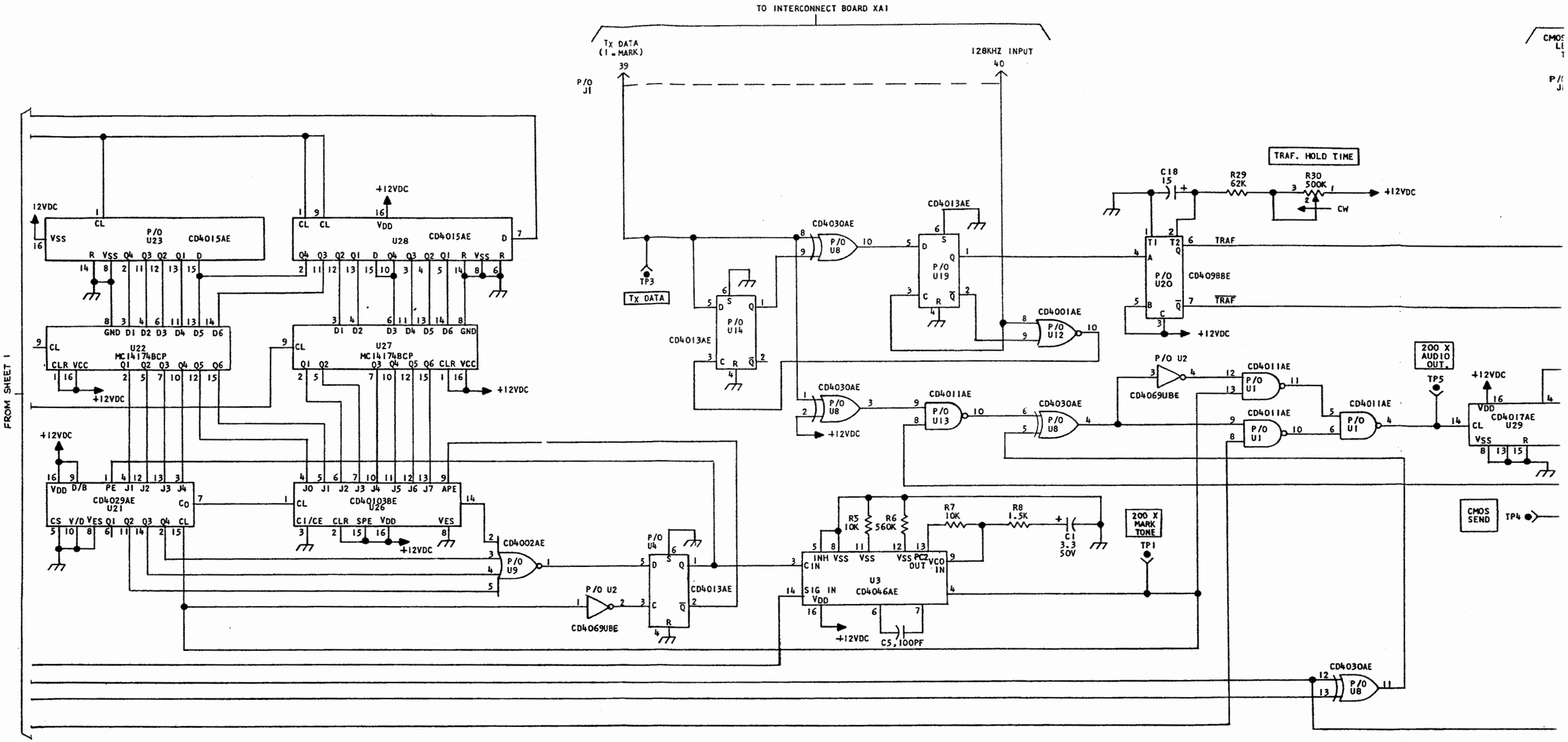

TO INTERCONNECT BOARD XA1
TX DATA (1=MARK)
39
128KHZ INPUT
40
P/O J1
FROM SHEET 1
TRAF. HOLD TIME
C18 15
R29 62K
R30 500K
CW
+12VDC
CD4030AE
CD4013AE
CD4001AE
CD4098BE
TRAF
TRAF
TP3
TX DATA
P/O U8
P/O U19
P/O U12
P/O U20
P/O U14
P/O U2
CD4069UBE
CD4011AE
P/O U13
P/O U1
200 X AUDIO OUT
TP5
CD4017AE U29
U22 MC14174BCP
U27 MC14174BCP
U21 CD4029AE
U26 CD40103BE
CD4002AE
P/O U9
P/O U4
R5 10K
R6 560K
R7 10K
R8 1.5K
C1 3.3 50V
200 X MARK TONE
TP1
U3 CD4046AE
C5, 100PF
CMOS SEND
TP4

Figure 7-2.

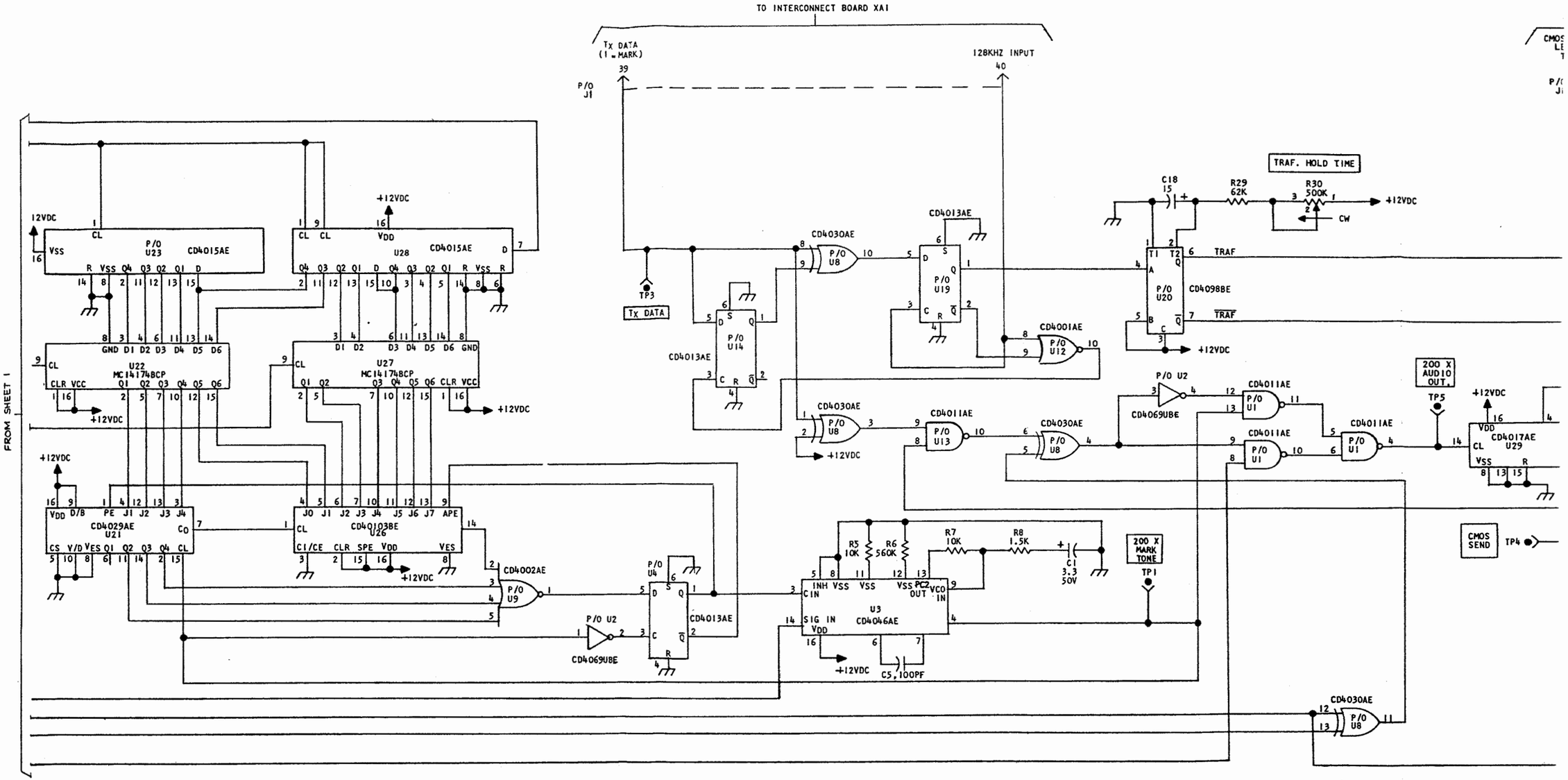

FROM SHEET 1
TO INTERCONNECT BOARD XA1
TX DATA (1 = MARK)
39
128KHZ INPUT
40
P/O J1
12VDC
+12VDC
VSS
VDD
CL
P/O U23
CD4015AE
U28
U22
MC14174BCP
U27
GND D1 D2 D3 D4 D5 D6
CLR VCC
Q1 Q2 Q3 Q4 Q5 Q6
U21
CD4029AE
VDD D/B PE J1 J2 J3 J4 CO
CS U/D VES Q1 Q2 Q3 Q4 CL
U26
CD40103BE
J0 J1 J2 J3 J4 J5 J6 J7 APE
C1/CE CLR SPE VDD VES
CD4002AE
P/O U9
TP3
TX DATA
CD4030AE
P/O U8
CD4013AE
P/O U14
P/O U19
CD4001AE
P/O U12
P/O U4
P/O U2
CD4069UBE
CD4011AE
P/O U13
P/O U1
TRAF. HOLD TIME
C18 15
R29 62K
R30 500K
CW
CD4098BE
P/O U20
TRAF
200 X AUDIO OUT.
TP5
CD4017AE
U29
R5 10K
R6 560K
R7 10K
R8 1.5K
C1 3.3 50V
200 X MARK TONE
TP1
U3
CD4046AE
INH VSS VSS VSS PC2 VCO OUT VCO IN
C IN
SIG IN
VDD
C5, 100PF
CMOS SEND
TP4
CD4030AE

Figure 7-2.

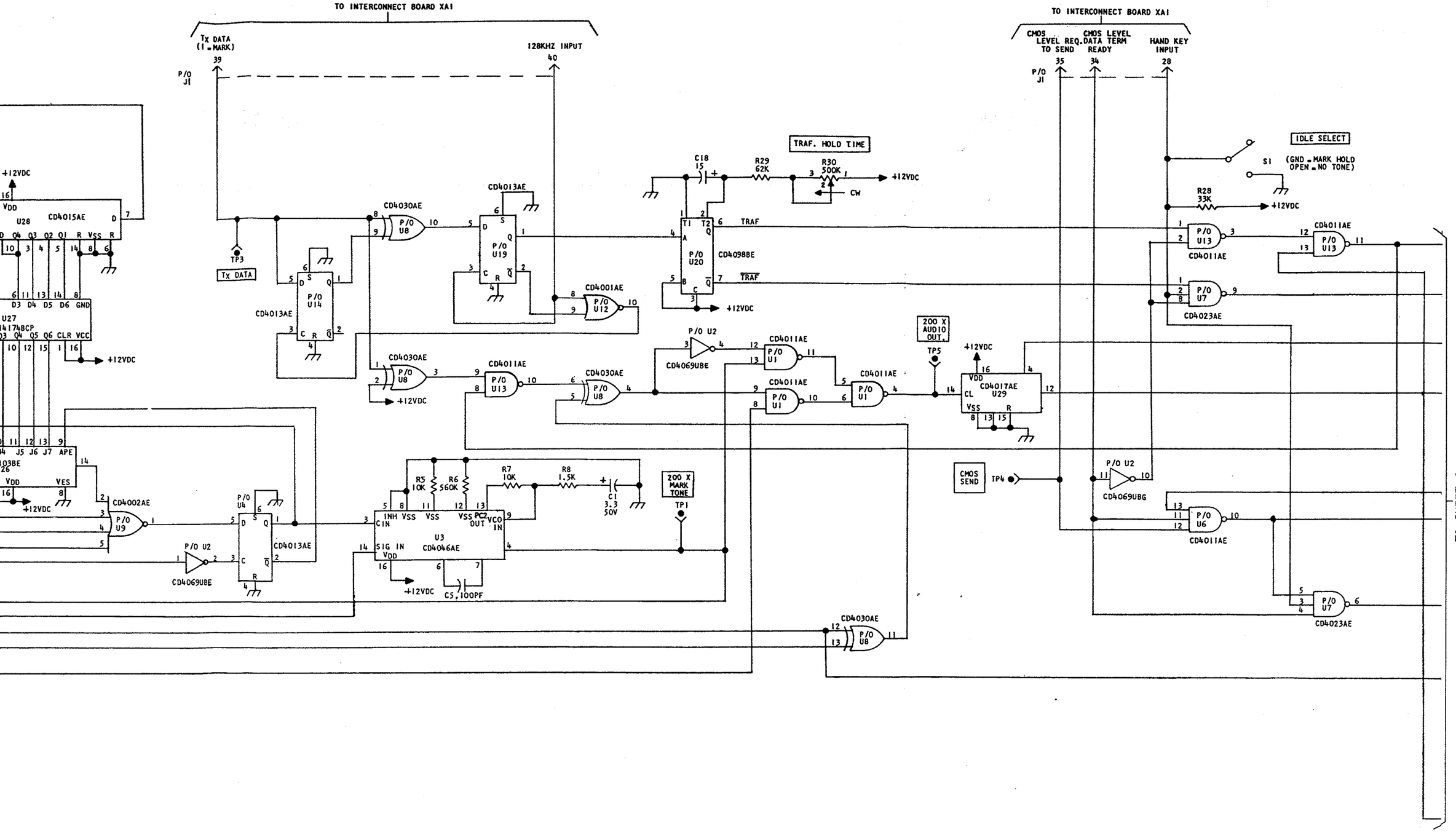


Figure 7-2. Modulator Pwb A1 Schematic Diagram (Sheet 2 of 4)

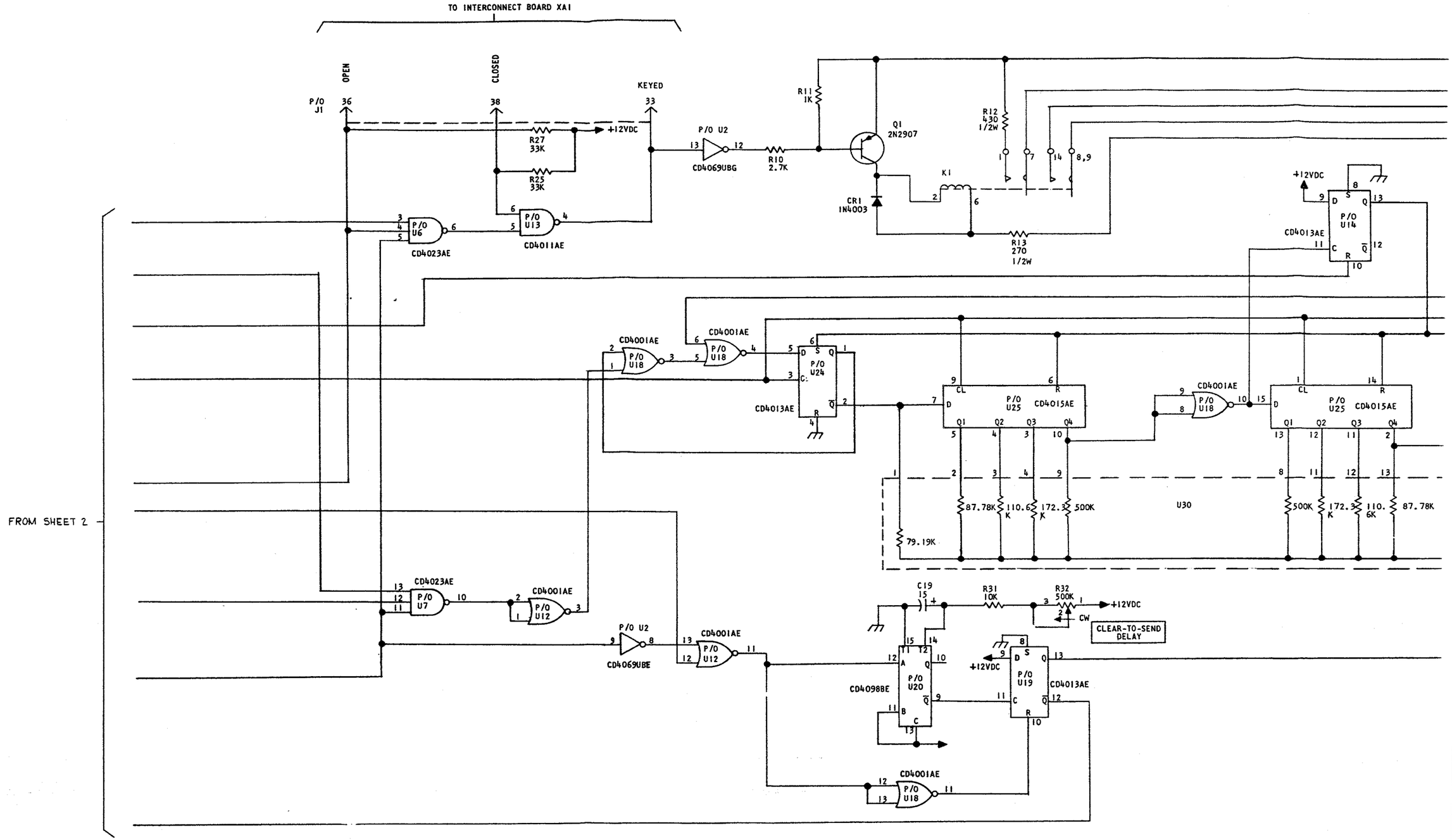

TO INTERCONNECT BOARD XA1
OPEN
CLOSED
KEYED
P/O J1
36
38
33
+12VDC
R27 33K
R25 33K
P/O U2
CD4069UBG
R10 2.7K
R11 1K
Q1 2N2907
R12 430 1/2W
K1
CR1 IN4003
R13 270 1/2W
P/O U6
CD4023AE
P/O U13
CD4011AE
+12VDC
P/O U14
CD4013AE
CD4001AE
P/O U18
P/O U24
CD4013AE
P/O U25
CD4015AE
U30
87.78K
110.6K
172.3K
500K
79.19K
500K
172.3K
110.6K
87.78K
FROM SHEET 2
P/O U7
CD4023AE
P/O U12
CD4001AE
P/O U2
CD4069UBE
C19
R31 10K
R32 500K
CW
+12VDC
CLEAR-TO-SEND DELAY
P/O U20
CD4098BE
P/O U19
CD4013AE

Figure 7-

TO INTERCONNECT BOARD XA1

CLOSED

KEYED

38

33

+12VDC

R27 33K

R25 33K

P/O U2

CD4069UBG

R10 2.7K

R11 1K

Q1 2N2907

R12 430 1/2W

1

7

14

8,9

K1

2

6

CR1 1N4003

R13 270 1/2W

P/O U6

CD4023AE

P/O U13

CD4011AE

+12VDC

P/O U14

CD4013AE

CD4001AE

P/O U18

P/O U24

CD4013AE

P/O U25 CD4015AE

CD4001AE

P/O U18

P/O U25 CD4015AE

P/O U24

CD4013AE

TO SHEET 4

87.78K

110.6 K

172.3 K

500K

U30

79.19K

500K

172.3 K

110. 6K

87.78K

79.19K

AUDIO OUT ADJ

CW

R18 5K

R14 100

P/O U31

HA1-4741-5

STEP SINUSOID

TP6

CD4023AE

P/O U7

CD4001AE

P/O U12

P/O U2

CD4069UBE

CD4001AE

P/O U12

C19

R31 10K

R32 500K

+12VDC

CW

CLEAR-TO-SEND DELAY

CD4098BE

P/O U20

+12VDC

P/O U19

CD4013AE

CD4001AE

P/O U18

Figure 7-2. Modulator Pwb A1 Schematic Diagram (Sheet 3 of 4)

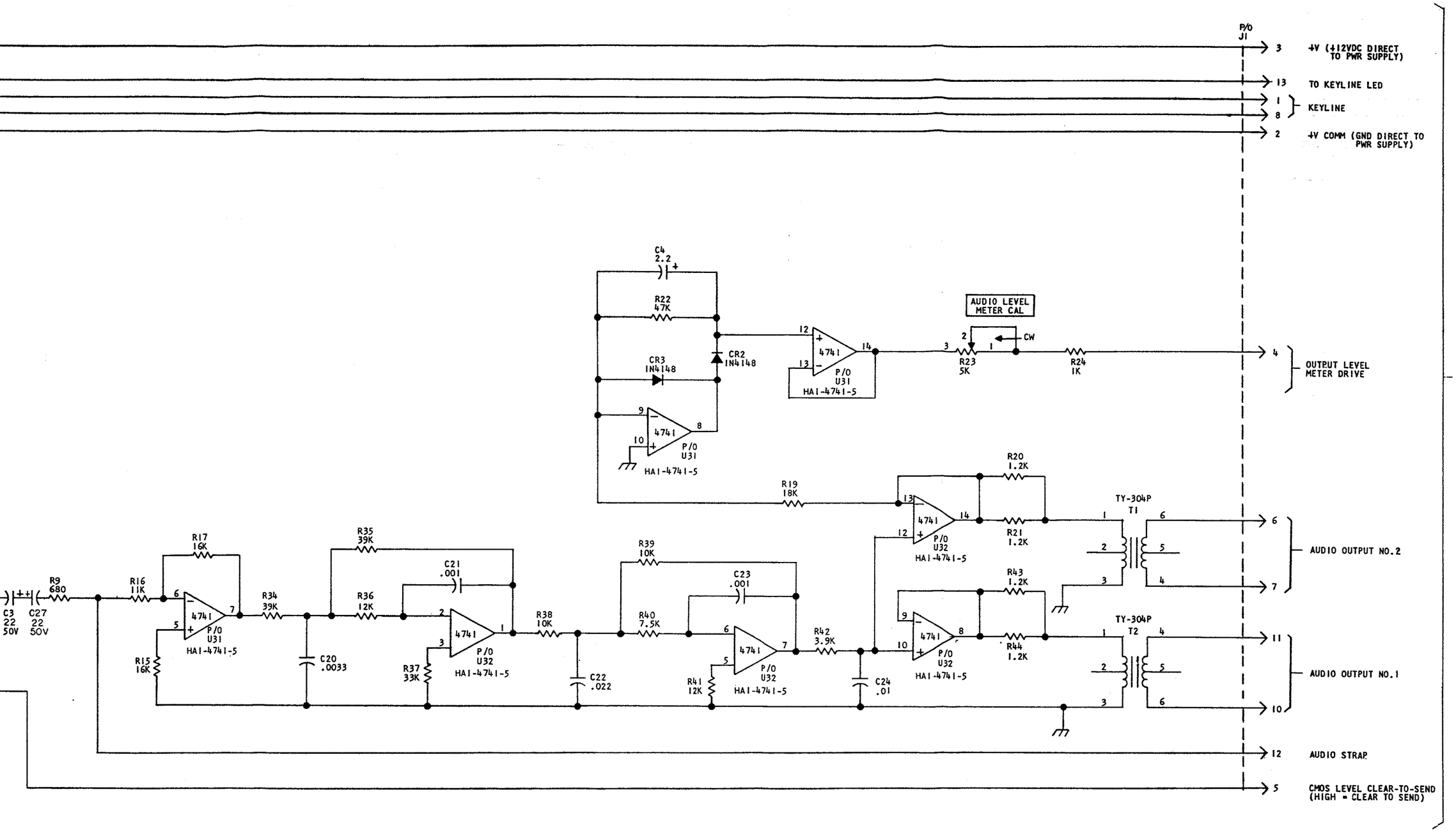


Figure 7-2. Modulator Pwb A1 Schematic Diagram (Sheet 4 of 4)

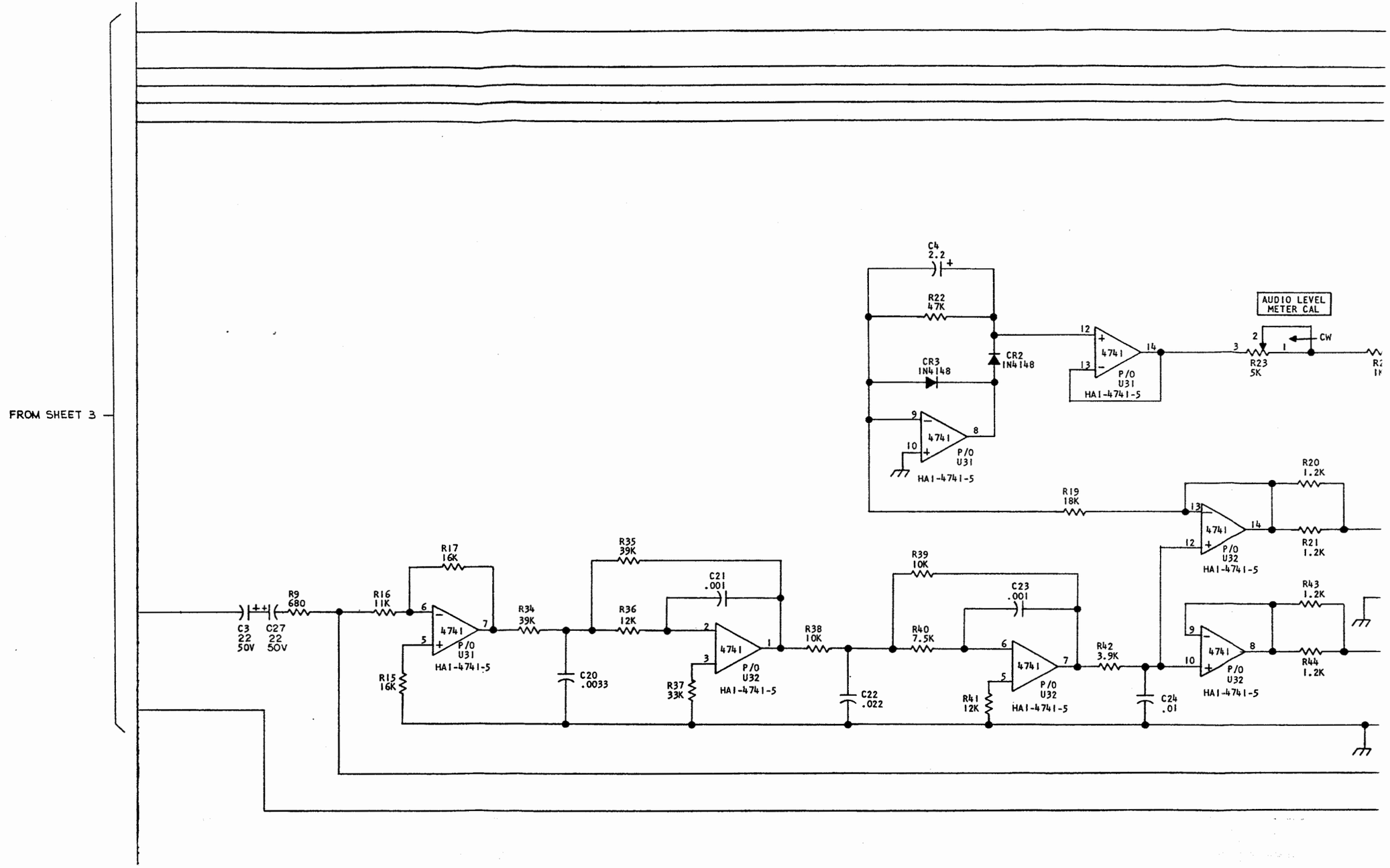

FROM SHEET 3
C4
2.2
R22
47K
CR3
IN4148
CR2
IN4148
4741
P/O
U31
HA1-4741-5
AUDIO LEVEL
METER CAL
CW
R23
5K
R19
18K
R20
1.2K
R21
1.2K
P/O
U32
HA1-4741-5
R43
1.2K
R44
1.2K
C3
22
50V
C27
22
50V
R9
680
R16
11K
R17
16K
R15
16K
R34
39K
R35
39K
R36
12K
C21
.001
R37
33K
C20
.0033
R38
10K
R39
10K
R40
7.5K
C23
.001
R41
12K
R42
3.9K
C22
.022
C24
.01

Figure 7-2.

NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTANCES ARE IN OHMS, ±5%, 1/4W, AND ALL CAPACITANCES ARE IN MICROFARADS.
2. CAPACITORS C65 THRU C80 ARE .0047UF.
3. J1 & J2 NOT USED ON RF-3352.

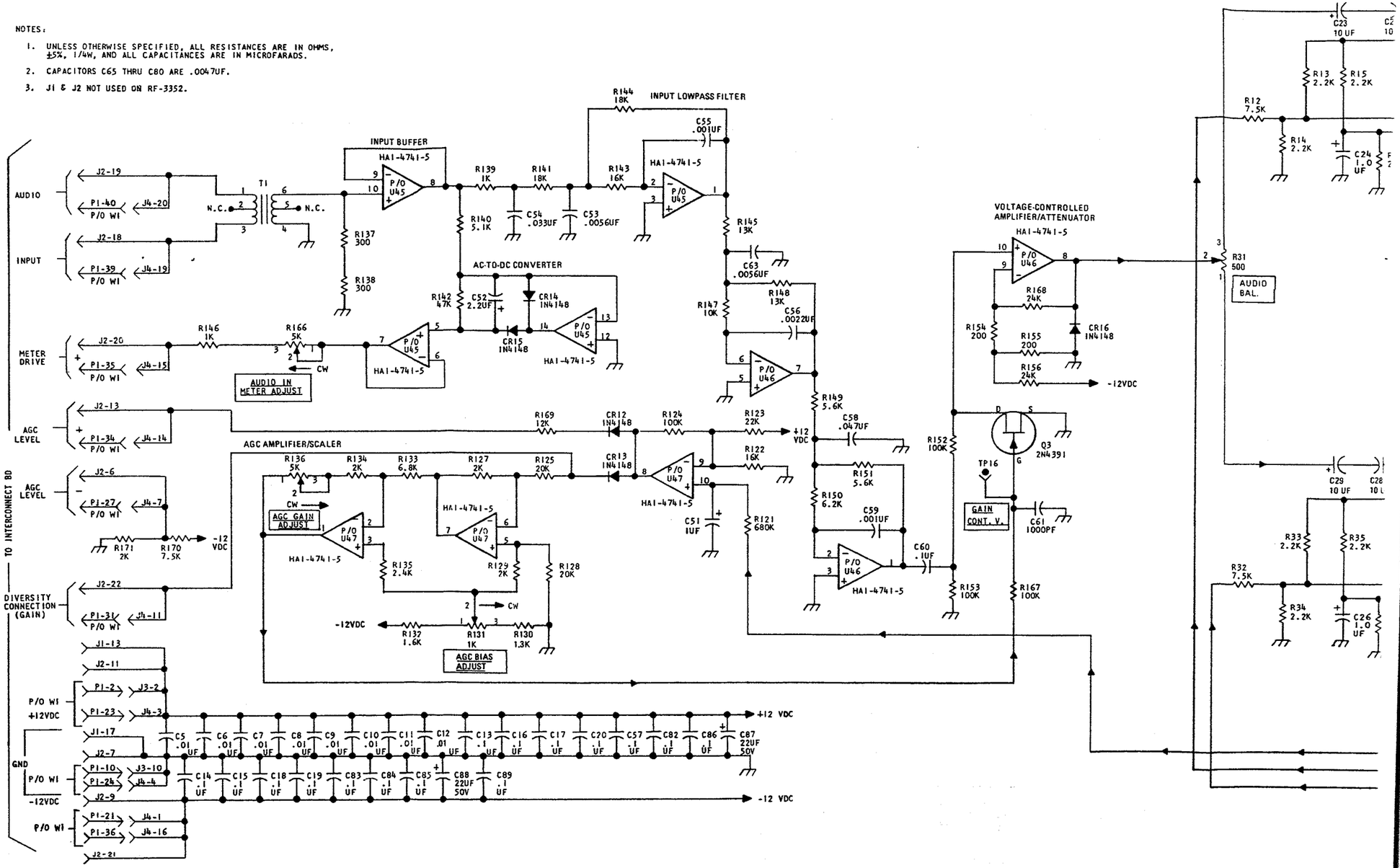


Figure 7-3.

FIED, ALL RESISTANCES ARE IN OHMS,
ACITANCES ARE IN MICROFARADS.
D ARE .0047UF.
-3352.

INPUT BUFFER
HA1-4741-5
INPUT LOWPASS FILTER
AC-TO-DC CONVERTER
AUDIO IN METER ADJUST
AGC AMPLIFIER/SCALER
AGC GAIN ADJUST
AGC BIAS ADJUST
GAIN CONT. V.
VOLTAGE-CONTROLLED AMPLIFIER/ATTENUATOR
AUDIO BAL.
MARK TONE MIXER
GAIN ADJ
MARK MIX. OUT
MARK MIX. BAL.
SPACE TONE MIXER
SPACE MIX. OUT
SPACE MIX. BAL.
+12 VDC
-12 VDC
-12VDC
CW

Figure 7-3. Demodulator Pwb A2 Schematic Diagram (Sheet 1 of 4)

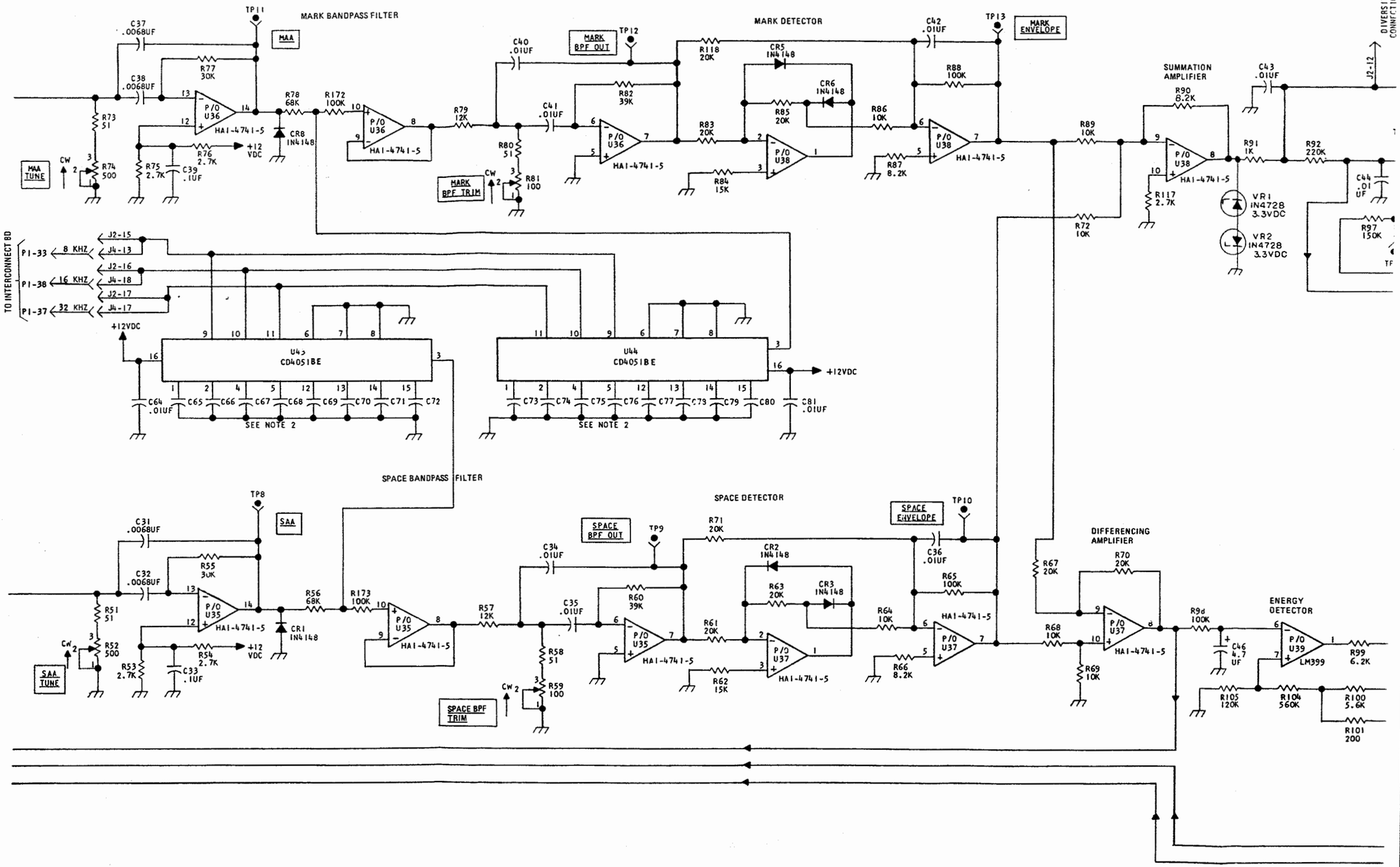

MARK BANDPASS FILTER
MARK DETECTOR
SUMMATION AMPLIFIER
DIVERSITY CONNECTION
MAA
MARK BPF OUT
MARK ENVELOPE
MAA TUNE
MARK BPF TRIM
TO INTERCONNECT BD
P1-33 8 KHZ
P1-38 16 KHZ
P1-37 32 KHZ
+12VDC
U43 CD4051BE
U44 CD4051BE
SEE NOTE 2
SPACE BANDPASS FILTER
SPACE DETECTOR
SAA
SPACE BPF OUT
SPACE ENVELOPE
SAA TUNE
SPACE BPF TRIM
DIFFERENCING AMPLIFIER
ENERGY DETECTOR
HA1-4741-5
LM399

Figure 7-3. De

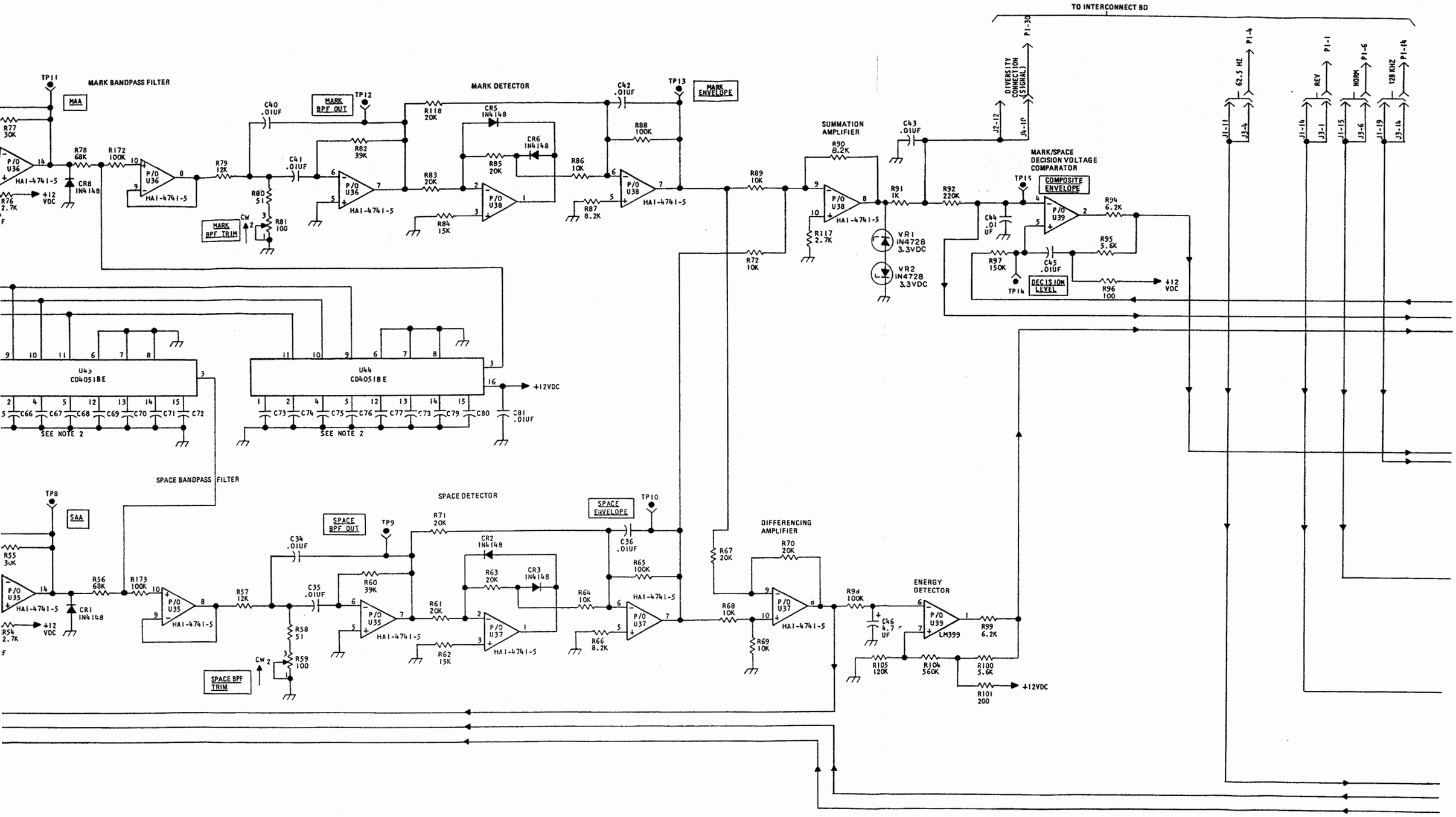


Figure 7-3. Demodulator Pwb A2 Schematic Diagram (Sheet 2 of 4)

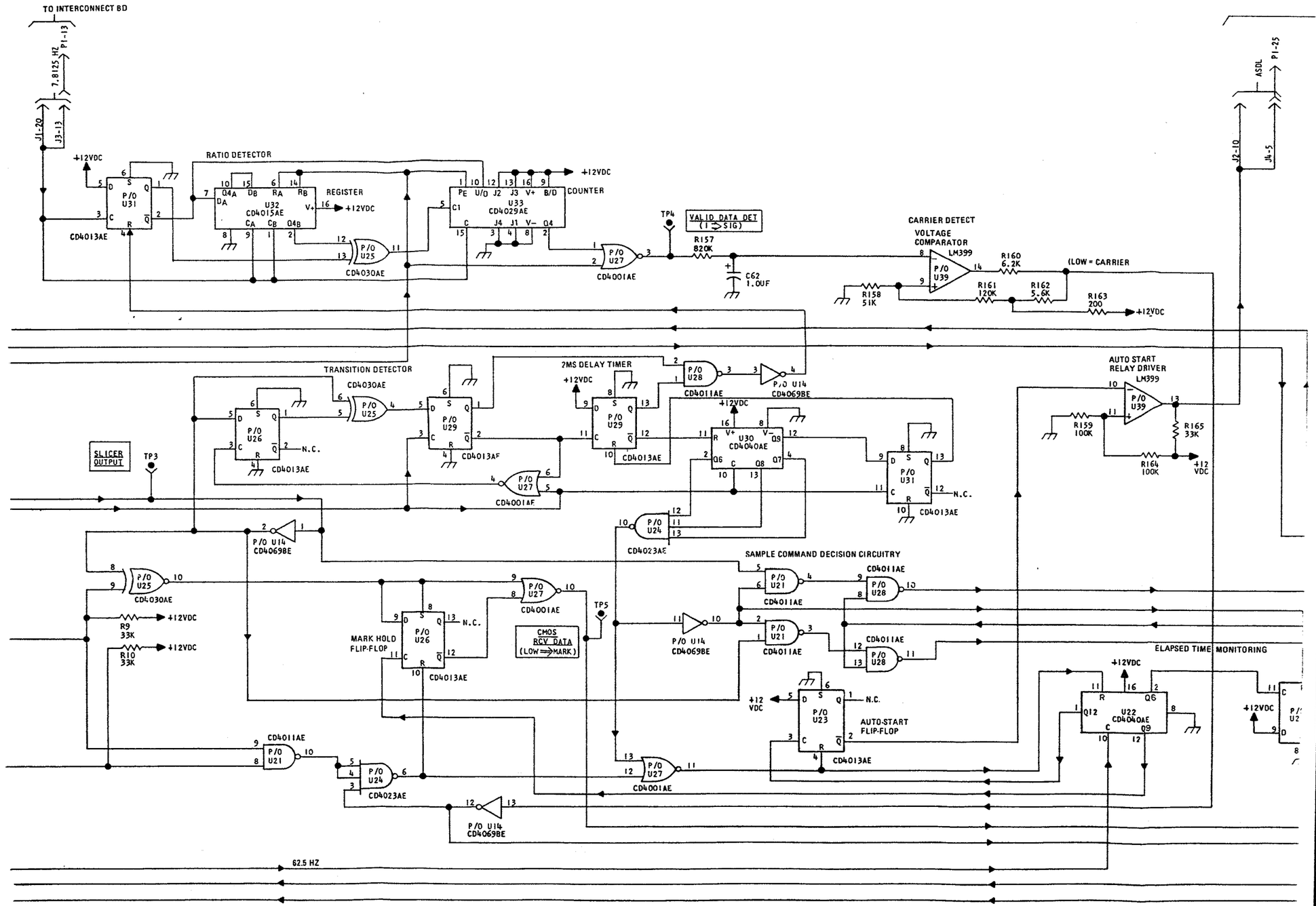

TO INTERCONNECT BD
7.8125 HZ
P1-13
J1-20
J3-13
+12VDC
RATIO DETECTOR
REGISTER
COUNTER
CD4013AE
CD4030AE
CD4029AE
CD4001AE
TP4
VALID DATA DET
(1 ⇒ SIG)
R157
820K
C62
1.0UF
CARRIER DETECT
VOLTAGE
COMPARATOR
LM399
R160
6.2K
R161
120K
R162
5.6K
R163
200
R158
51K
(LOW = CARRIER
ASDL
P1-25
J2-10
J4-5
TRANSITION DETECTOR
2MS DELAY TIMER
CD4011AE
CD4069BE
CD4040AE
CD4023AE
AUTO START
RELAY DRIVER
R159
100K
R164
100K
R165
33K
+12
VDC
SLICER
OUTPUT
TP3
N.C.
P/O U14
P/O U21
P/O U23
P/O U24
P/O U25
P/O U26
P/O U27
P/O U28
P/O U29
P/O U30
P/O U31
P/O U39
R9
33K
R10
33K
MARK HOLD
FLIP-FLOP
CMOS
RCV DATA
(LOW⇒MARK)
TP5
SAMPLE COMMAND DECISION CIRCUITRY
AUTO-START
FLIP-FLOP
ELAPSED TIME MONITORING
U22
62.5 HZ

Figure 7-3. D

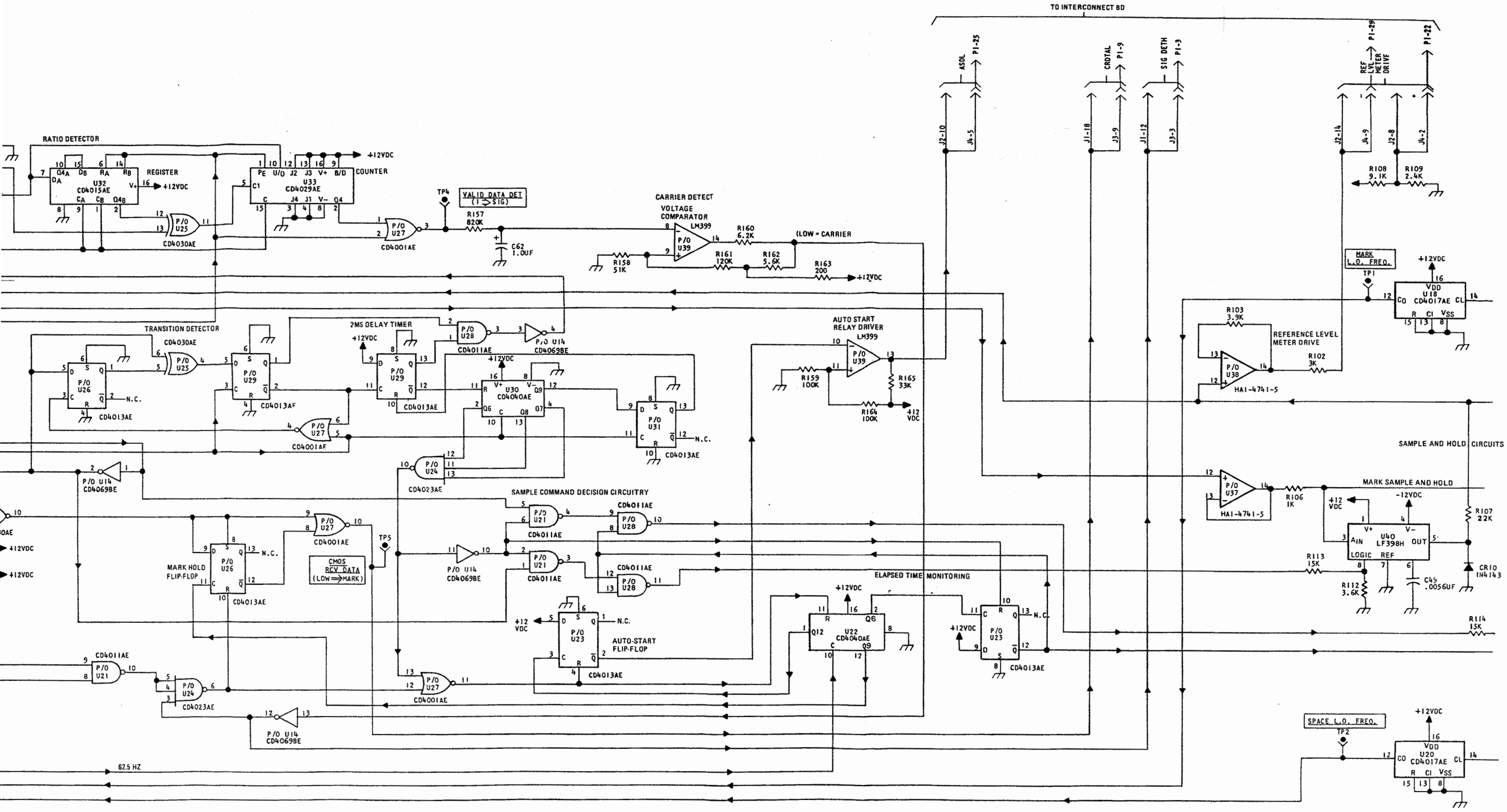


Figure 7-3. Demodulator Pwb A2 Schematic Diagram (Sheet 3 of 4)

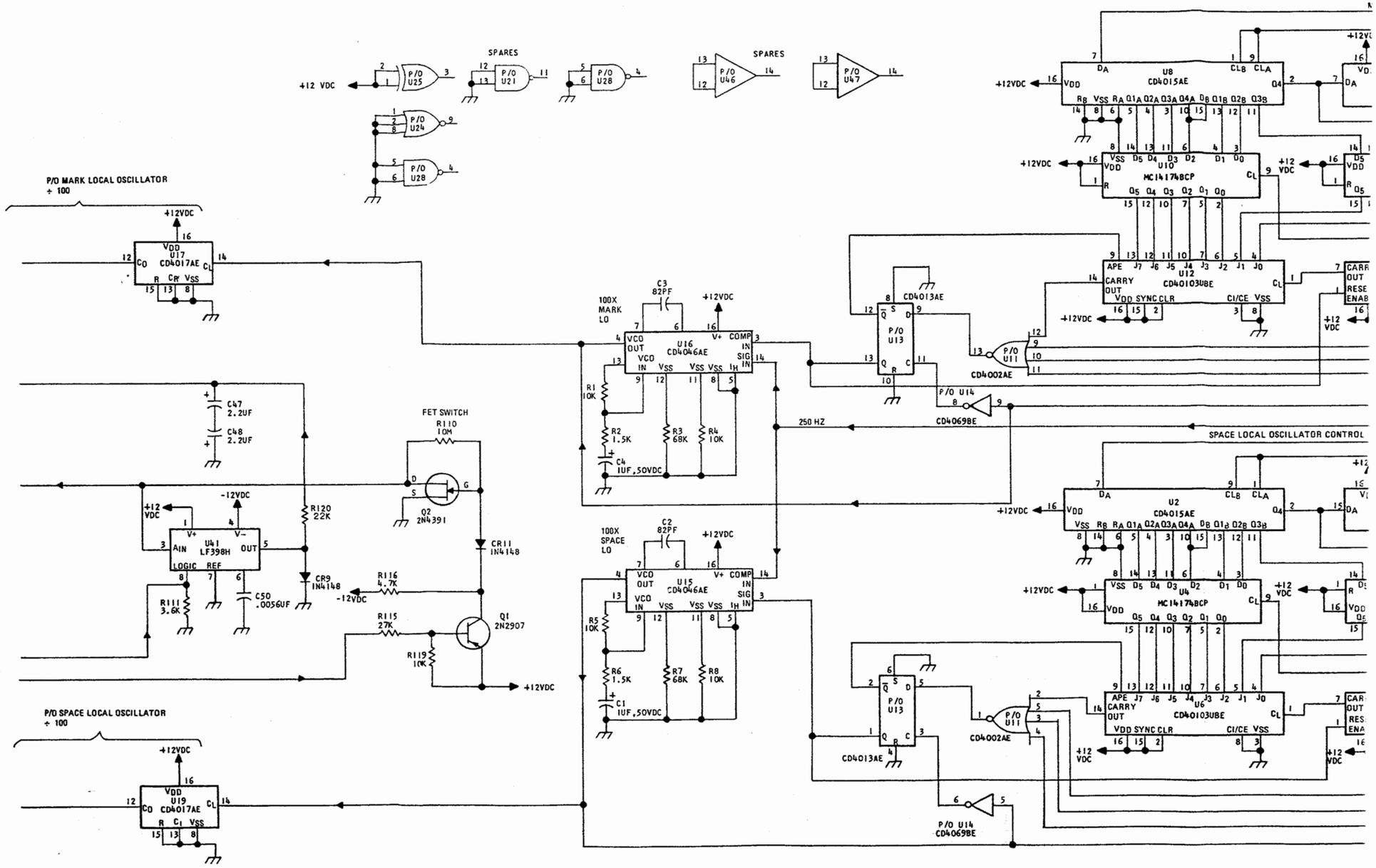

SPARES
SPARES
+12 VDC
P/O U25
P/O U21
P/O U28
P/O U24
P/O U28
P/O U46
P/O U47
P/O MARK LOCAL OSCILLATOR
÷ 100
+12VDC
U17
CD4017AE
C47
2.2UF
C48
2.2UF
FET SWITCH
R110
10M
Q2
2N4391
-12VDC
R120
22K
U41
LF398H
CR9
IN4148
C50
.0056UF
R111
3.6K
R116
4.7K
R115
27K
R119
10K
CR11
IN4148
Q1
2N2907
P/O SPACE LOCAL OSCILLATOR
÷ 100
U19
CD4017AE
100X
MARK
LO
C3
82PF
U16
CD4046AE
R1
10K
R2
1.5K
C4
1UF,50VDC
R3
68K
R4
10K
100X
SPACE
LO
C2
82PF
U15
CD4046AE
R5
10K
R6
1.5K
C1
1UF,50VDC
R7
68K
R8
10K
CD4013AE
P/O U13
CD4002AE
P/O U11
CD4069BE
P/O U14
250 HZ
SPACE LOCAL OSCILLATOR CONTROL
U8
CD4015AE
U10
MC14174BCP
U12
CD4010J3UBE
U2
CD4015AE
U4
MC14174BCP
U6
CD4010J3UBE

Figure 7-3. D

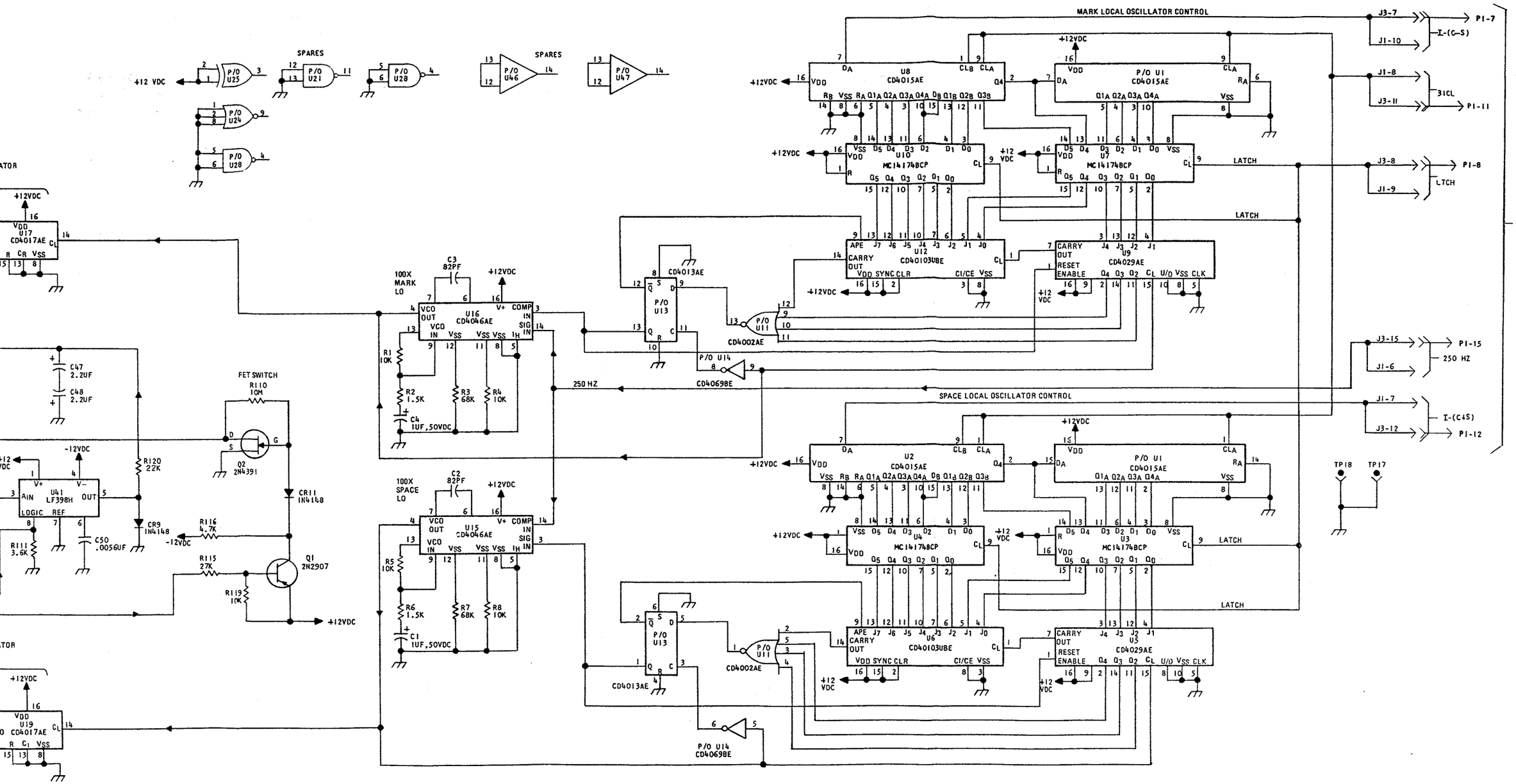


Figure 7-3. Demodulator Pwb A2 Schematic Diagram (Sheet 4 of 4)

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
   B. ALL CAPACITORS ARE IN MICROFARADS, 50V.

TO INTERCONNECT XA3

CFUN5 CFTN2 CFTN8 CFTN1 CFTN4 CFH2 CFH8 CFTH2 CFH1 CFH4 CFTH1

P/O J1

P/O U9 33K +12VDC

P/O U1 33K +12VDC

P/O U9 33K

P/O U1 33K +12VDC

U5 CD4029 (J1 J2 J3 J4 VDD CO CE V/D D/B VE CS CL PE)

U2 CD40102 (J0 J1 J2 J3 J4 J5 J6 J7 CO CE PRE CL VSS VDD PRE CLR)

P/O U1 33K

U20 Q-TECH QT3 1.024 MHZ

TP1 OSC OUT

U19 CD4024 (VDD Q3 Q4 Q5 Q6 Q7 IP VSS R)

TP2 8 KHZ

U15 CD4024 (VDD Q4 Q5 Q7 IP VSS R Q3)

1000 HZ

U16 CD4024 (VDD IP Q4 Q2 Q1 Q5)

P/O U6 CD4023

U8 CD4040 (R VDD INPUT Q12 Q11 Q10 Q9 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1)

U3 CD4021 (SI VSS Q8 CL PSC)

U4 CD4021 (SI VSS Q8 CL PSC VDD)

TO INTERCONNECTION BOARD XA3

+12VDC 19,22 — C1 22 C2 .01 C3 .01 C4 .01 C5 .01 C6 .01 C7 .01 — +12VDC

COMMON 20,21

SHH4 13

SHTN1 12

SHH1 14

SHTN8 15

SHTN4 16

SHTN2 18

SHTN1 17

SHUTM 24 — R2 33K — +12VDC

SHUTL 25 — R1 33K

P/O U9 33K +12 VDC

U10 CD40102 (J0 J1 J2 J3 J4 J5 J6 J7 CO CE VSS PRE CE VDD PRE CLR)

P/O U6 CD4023

U12 CD4021 (SI VDD CL PS6 Q8 VSS)

U7 CD4024 (Q7 Q6 Q5 Q4 Q3 Q2 Q1 VDD IP R VSS)

U11 CD4032 (A1 B1 A2 B2 B3 CR A3 CL)

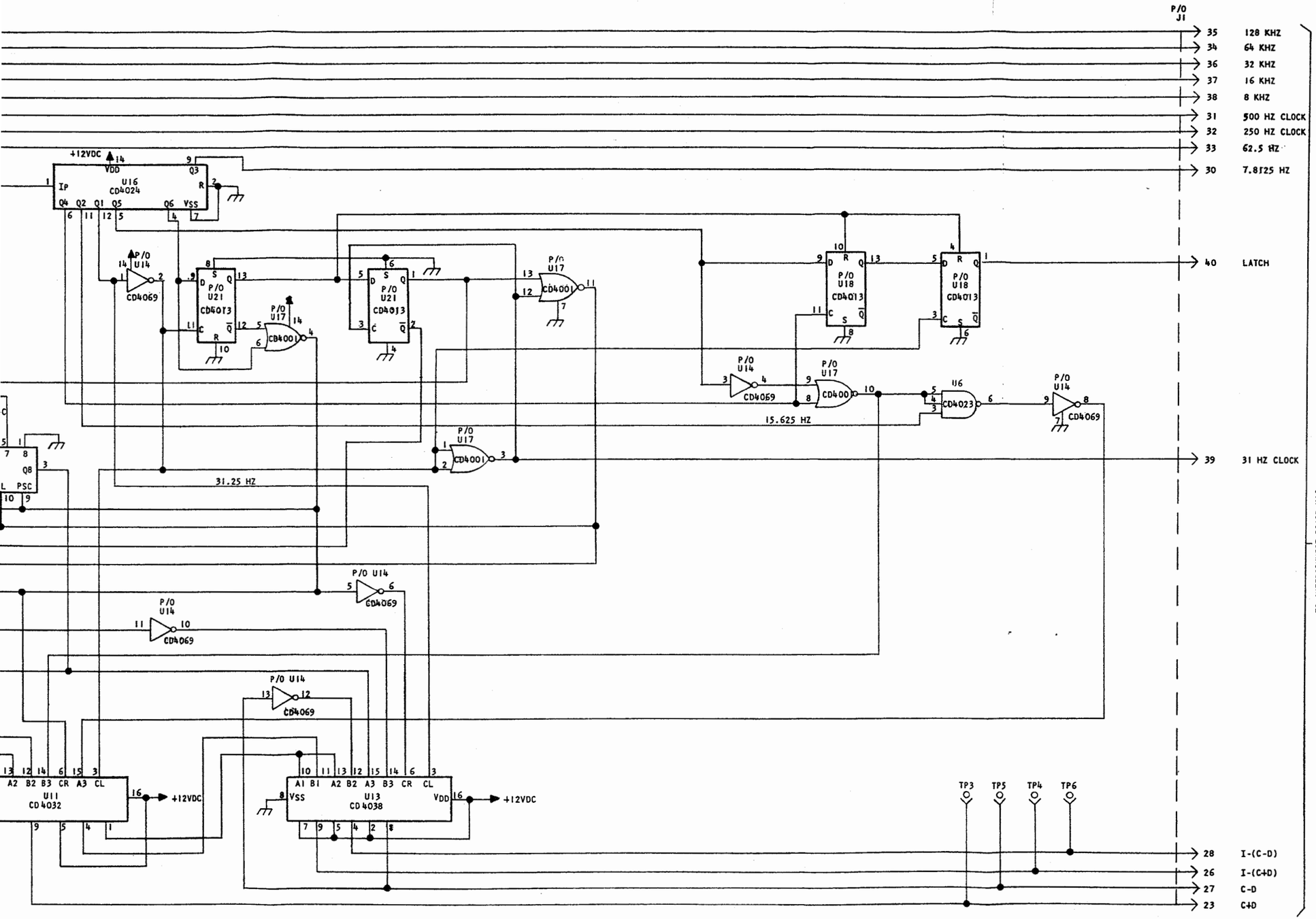


Figure 7-4. Timing and Control Pwb A3 Schematic Diagram

TO INTERCONNECT BD XA4

TRANSMIT

DATA IN

J1/3 XA4 P/O J1

J1/2

J1/8

J1/4

INPUT LOOP METER CAL. ADJ.

P/O J1 TO METER

R1 1K CW

R2 4.7

R3 6.8

R4 10K

Q1 2N6515

L1 220UH

U1 VM28

C1 3300PF 500V

R5 30K 1W

R6 270 1W

R7 120 1/2W

R8 120 1/2W

R9 2K

R10 2K

C2 .1

+12VDC

P/O U4 CD4011AE

U2 4N35

U3 4N35

P/O U4 CD4011AE

P/O U4 CD4011AE

U5 MC14539CP

+12VDC

NEUTRAL

S1

POLAR

+12VDC

R33 33K

R34 33K

CD4011AE P/O U4

S2

PSDTR

U8 MC1489L

P/O U9 CD4069BE

DATA TERMINAL READY 20

TRANSMITTED DATA 21

REQUEST TO SEND 19

+12VDC INPUT 28

COMMON 27

-12VDC INPUT 26

+65VDC IN 23

-65VDC IN 24

C12 22 50V

C13 22 50V

C9 .1

+12VDC

-12VDC

CR6 IN4003

CR7 IN4003

DRIVER A

DRIVER B

+12VDC

R14 680

U10 4N35

P/O U6 CD4049BE

R16 270K

R17 20K

R18 2.2K

R19 10K 2W

Q2 2N6518

Q4 2N6515

R35 120K

CR8 IN4003

CR10 IN4003

P/O U9 CD4069BE

P/O U6 CD4049BE

U11 4N35

R15 680

R20 10K 2W

Q3 2N6515

Q5 2N6518

R21 270K

R22 20K

R23 2.2K

R24 120K

CR9 IN4003

CR11 IN4003

OUTPUT LOOP METER CAL. ADJ.

CW

R25 1K

R26 4.7

R27 6.8

R28 10K

R29 30K 1W

R36 22 1/2W

CR13 IN4003

C11 3300PF 500V

C10 3300PF 500V

Q6 2N6515

CR12 IN4003

TO SHEET 2

-METOUT

T.T.Y DRIVE J1/9 (RCV)

+METOUT

OLPT OUT

OLPT FB

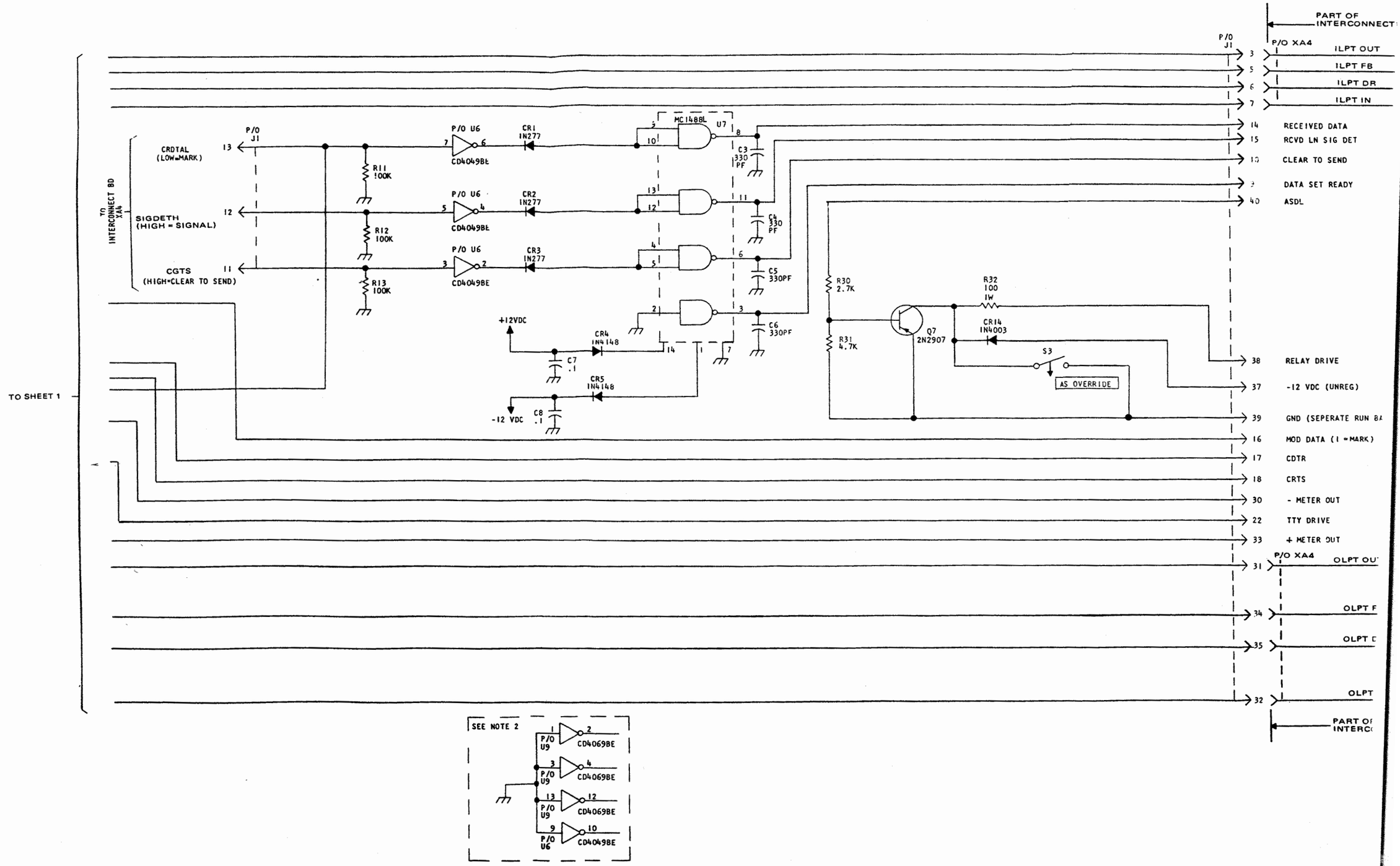
OLPT DR

OLPT IN

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTANCES ARE IN OHMS, ±5%, 1/4W.
   B. ALL CAPACITANCES ARE IN MICROFARADS.
2. THESE COMPONENTS ARE NON-FUNCTIONING PARTS OF THE IC'S SPECIFIED.
3. [ ] INDICATES PWB MARKING
4. PREFIX ALL PARTIAL REFERENCE DESIGNATIONS WITH A4.

Figure 7-5. Interface Pwb A4 Schematic Diagram (Sheet 1 of 2)


TO SHEET 1
TO INTERCONNECT BD XA4
CRDTAL (LOW=MARK)
SIGDETH (HIGH = SIGNAL)
CGTS (HIGH=CLEAR TO SEND)
P/O J1
13
12
11
R11 100K
R12 100K
R13 100K
P/O U6
CD4049BE
CR1 IN277
CR2 IN277
CR3 IN277
MC1488L
U7
C3 330 PF
C4 330 PF
C5 330PF
C6 330PF
+12VDC
-12 VDC
CR4 IN4148
CR5 IN4148
C7 .1
C8 .1
R30 2.7K
R31 4.7K
R32 100 1W
Q7 2N2907
CR14 IN4003
S3
AS OVERRIDE
PART OF INTERCONNECT
P/O XA4
ILPT OUT
ILPT FB
ILPT DR
ILPT IN
RECEIVED DATA
RCVD LN SIG DET
CLEAR TO SEND
DATA SET READY
ASDL
RELAY DRIVE
-12 VDC (UNREG)
GND (SEPERATE RUN BA
MOD DATA (1 = MARK)
CDTR
CRTS
- METER OUT
TTY DRIVE
+ METER OUT
OLPT OU
OLPT F
OLPT D
OLPT
PART OF INTERC
SEE NOTE 2
P/O U9
CD4069BE
P/O U6
CD4049BE

Figure

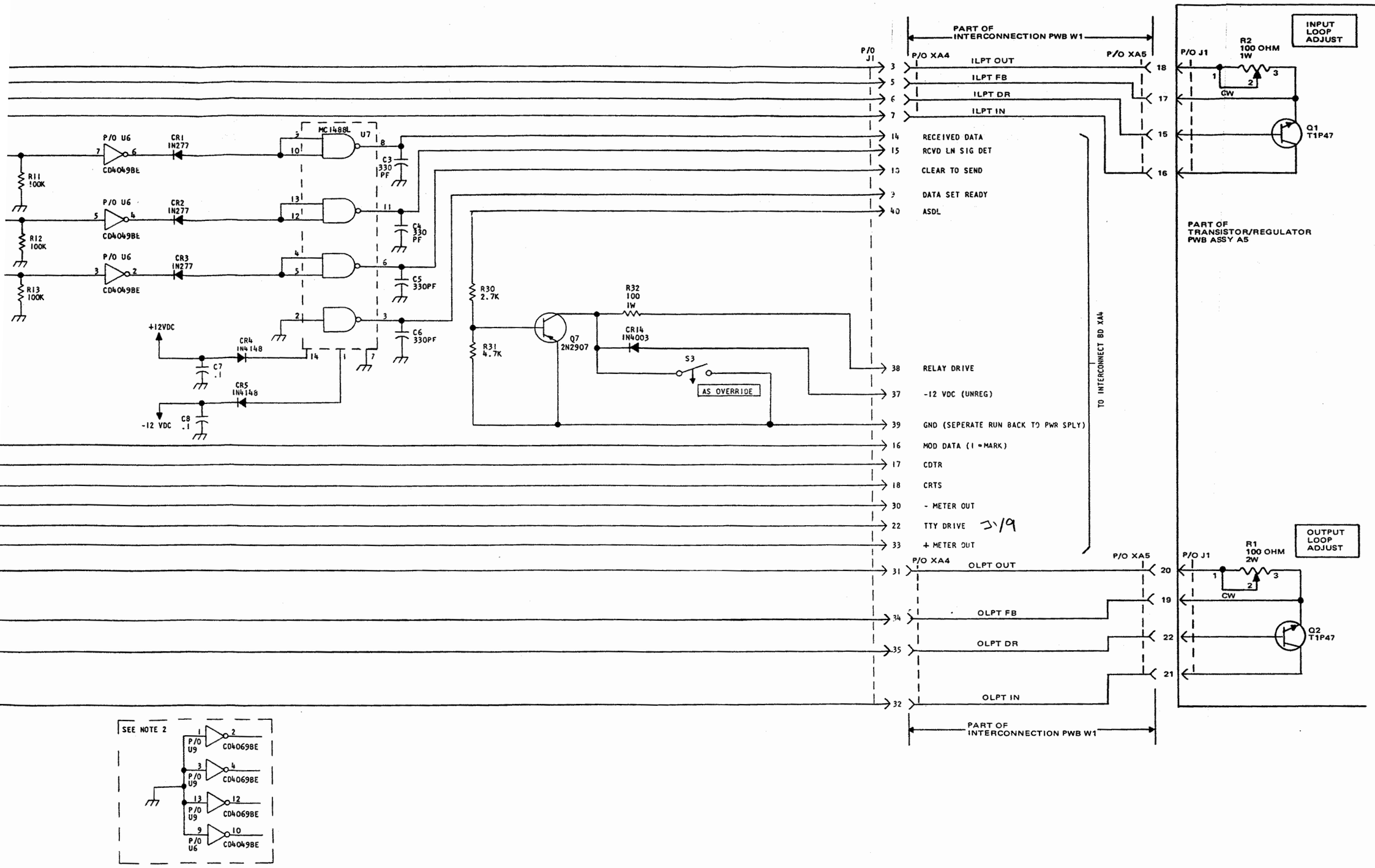


Figure 7-5. Interface Pwb A4 Schematic Diagram (Sheet 2 of 2)

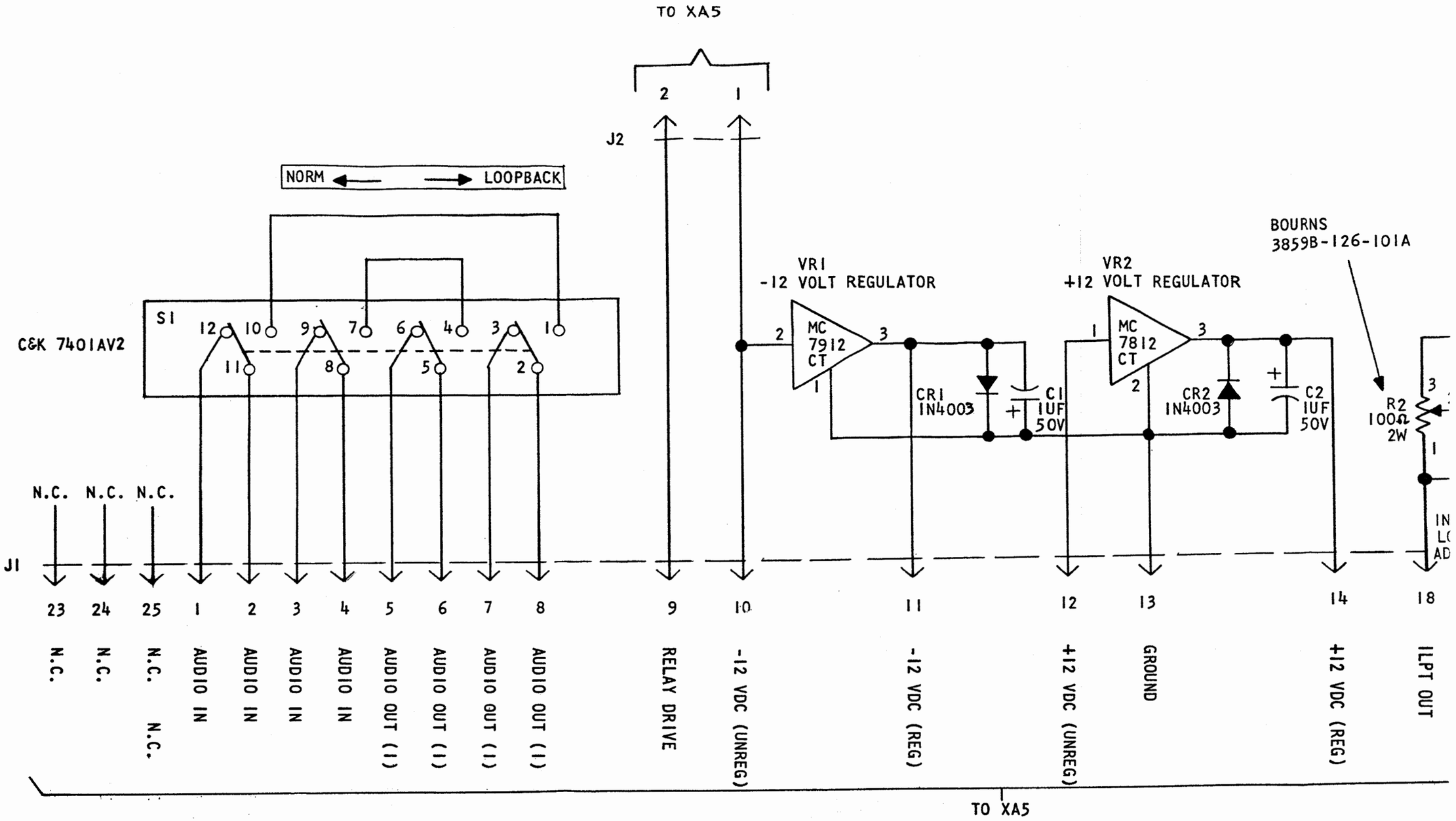

TO XA5
2
1
J2
NORM
LOOPBACK
S1
C&K 7401AV2
12
10
9
7
6
4
3
1
11
8
5
2
VR1
-12 VOLT REGULATOR
MC
7912
CT
CR1
IN4003
C1
1UF
50V
VR2
+12 VOLT REGULATOR
MC
7812
CT
CR2
IN4003
C2
1UF
50V
BOURNS
3859B-126-101A
R2
100Ω
2W
N.C.
N.C.
N.C.
J1
23 N.C.
24 N.C.
25 N.C.
1 AUDIO IN
2 AUDIO IN
3 AUDIO IN
4 AUDIO IN
5 AUDIO OUT (1)
6 AUDIO OUT (1)
7 AUDIO OUT (1)
8 AUDIO OUT (1)
9 RELAY DRIVE
10 -12 VDC (UNREG)
11 -12 VDC (REG)
12 +12 VDC (UNREG)
13 GROUND
14 +12 VDC (REG)
18 ILPT OUT
TO XA5

Figure 7-6.

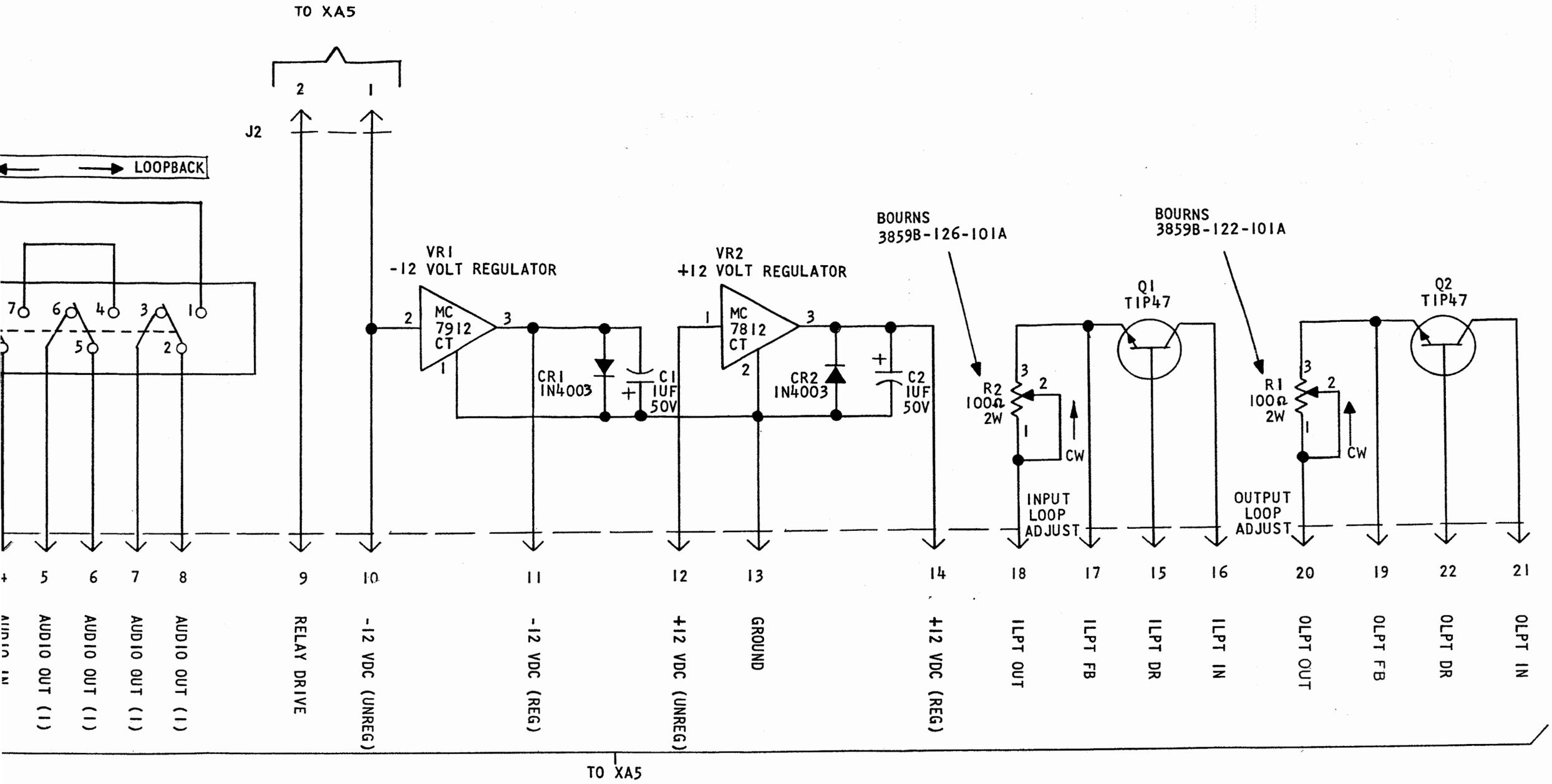
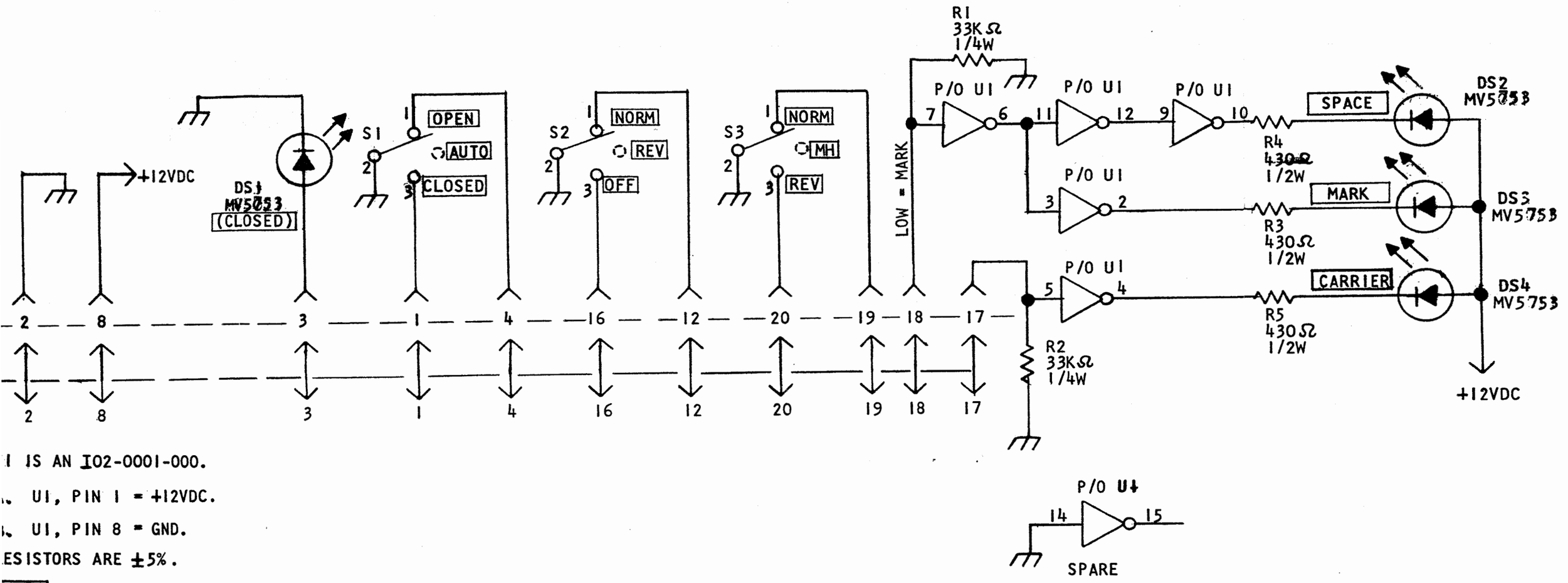


Figure 7-6. Transistor/Regulator Pwb A5 Schematic Diagram



1 IS AN I02-0001-000.

. U1, PIN 1 = +12VDC.

. U1, PIN 8 = GND.

ESISTORS ARE ±5%.

☐ INDICATES FRONT PANEL MARKING.

REFIX ALL REFERENCE DESIGNATORS WITH A6.

Figure 7-7. Control and Indicator Pwb A6 Schematic Diagram

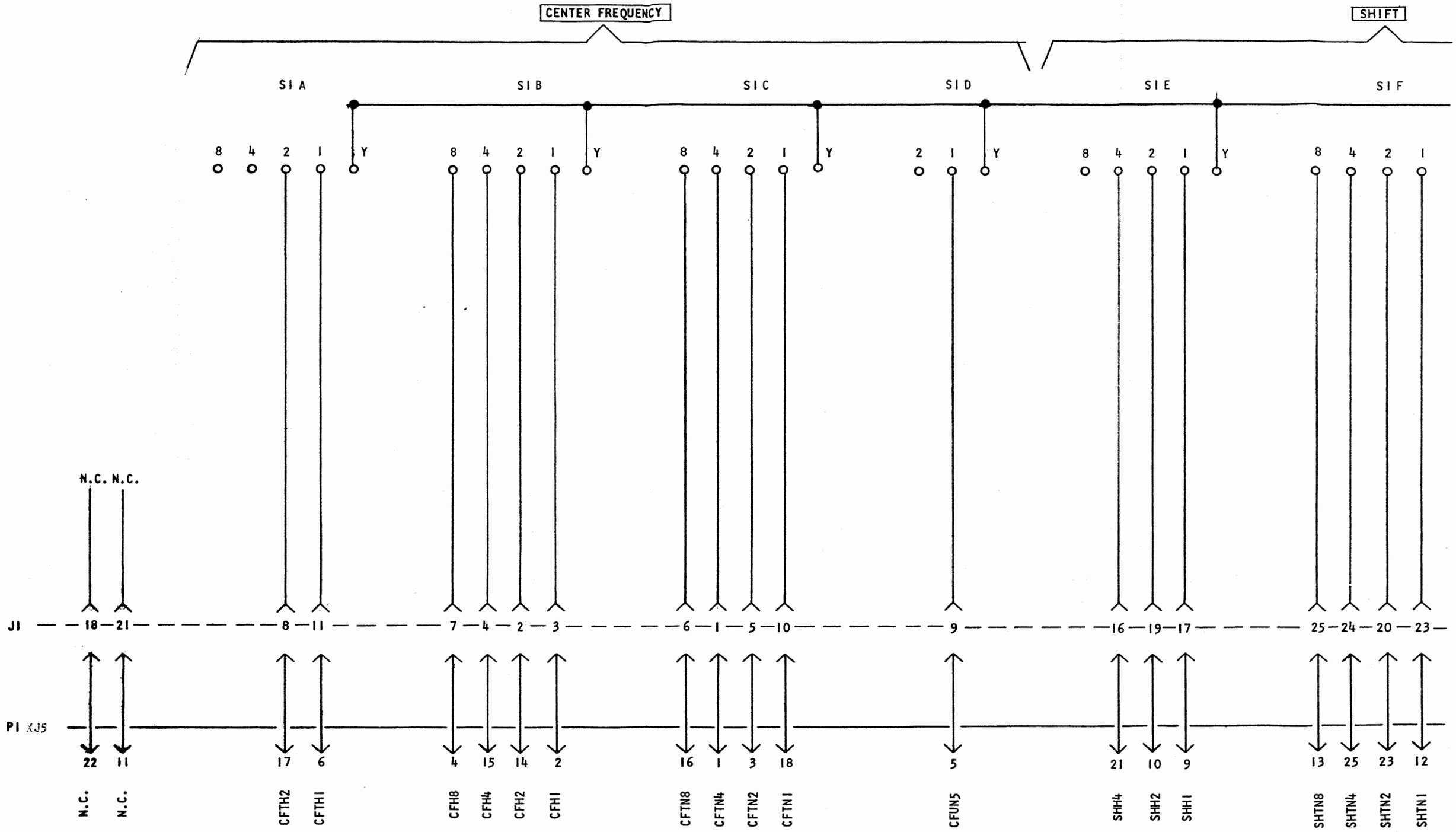

CENTER FREQUENCY
SHIFT
SI A
SI B
SI C
SI D
SI E
SI F
8 4 2 1 Y
8 4 2 1 Y
8 4 2 1 Y
2 1 Y
8 4 2 1 Y
8 4 2 1
N.C. N.C.
J1 — 18 — 21 — — — — — — — 8 — 11 — — — 7 — 4 — 2 — 3 — — — — 6 — 1 — 5 — 10 — — — — — — 9 — — — — — 16 — 19 — 17 — — — 25 — 24 — 20 — 23 —
P1 XJ5
22 11 17 6 4 15 14 2 16 1 3 18 5 21 10 9 13 25 23 12
N.C. N.C. CFTH2 CFTH1 CFH8 CFH4 CFH2 CFH1 CFTN8 CFTN4 CFTN2 CFTN1 CFUN5 SHH4 SHH2 SHH1 SHTN8 SHTN4 SHTN2 SHTN1

Figure 7-8. Fr

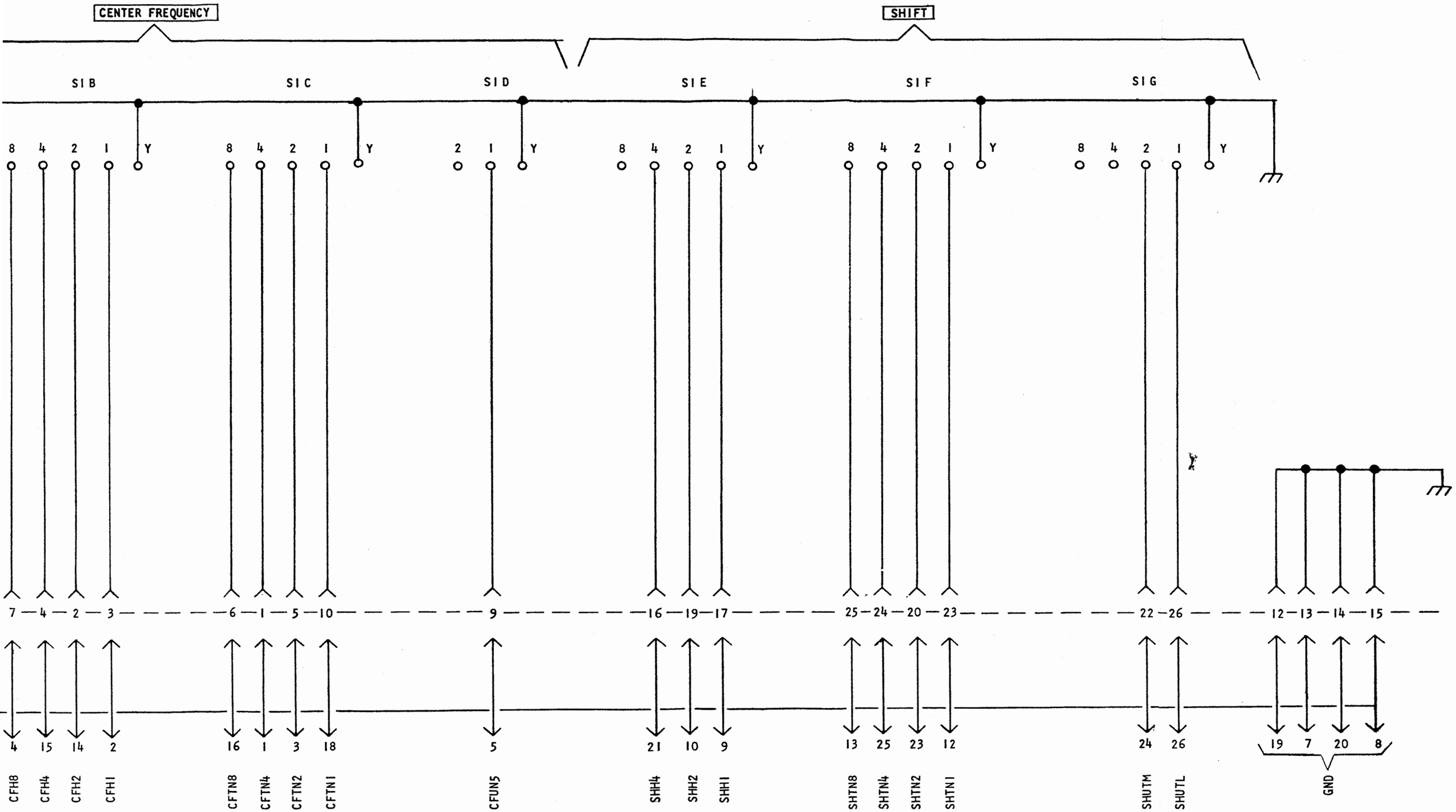


Figure 7-8. Frequency Control Board Assembly A7 Schematic Diagram

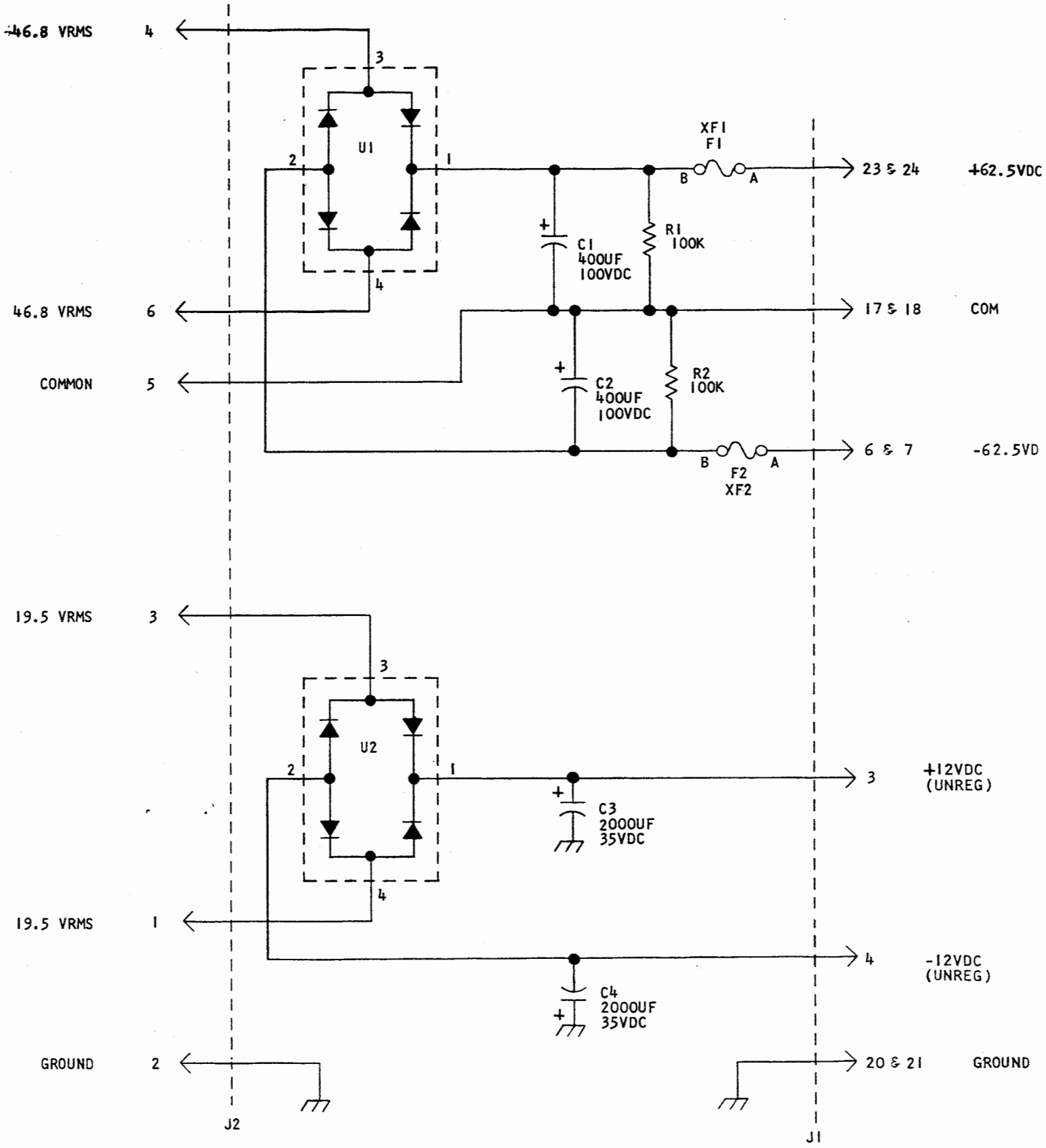


Figure 7-9. Power Supply Pwb PS1 Schematic Diagram

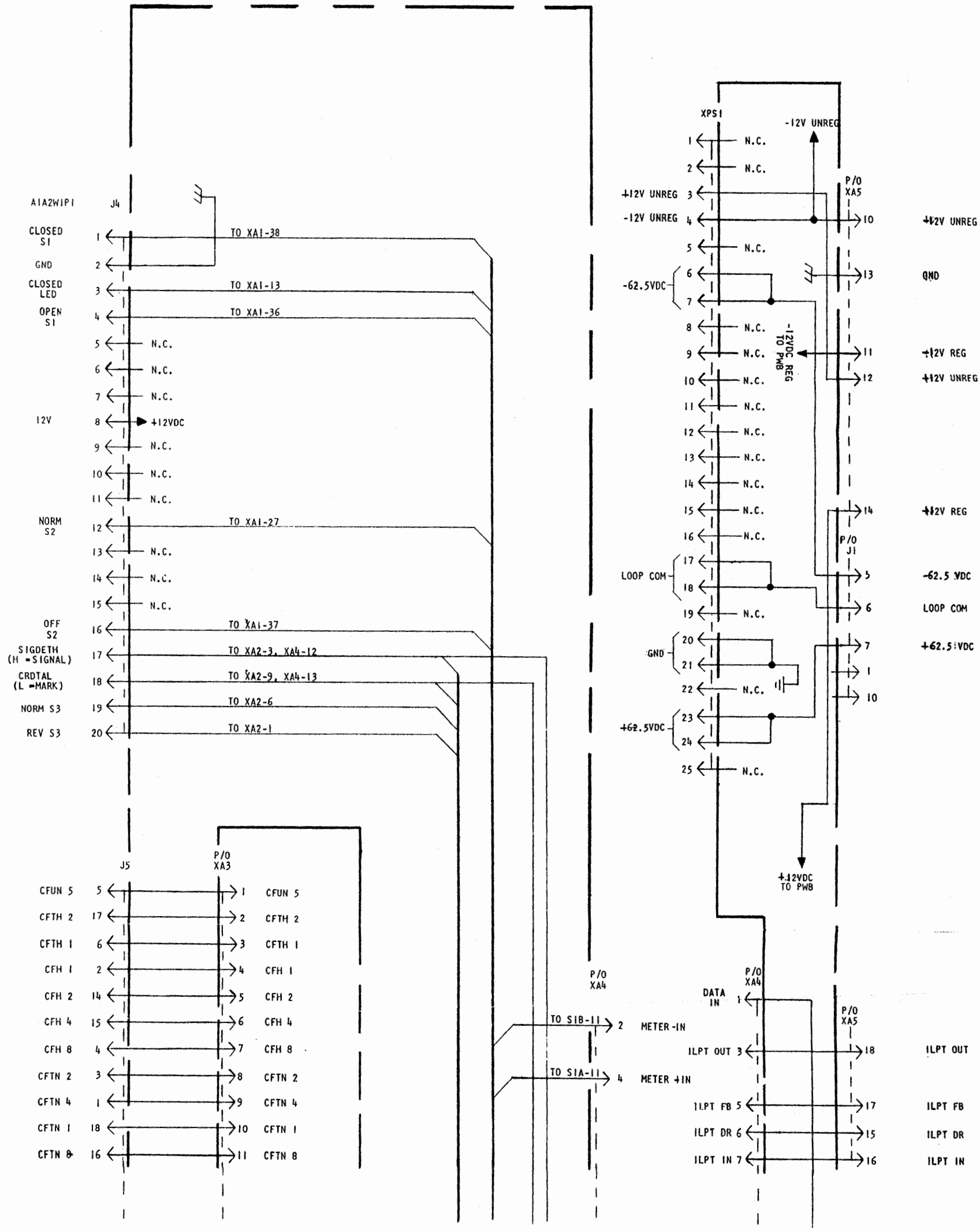


Figure 7-10. Interconnection Pwb W1 Schematic Diagram (Sheet 1 of 3)

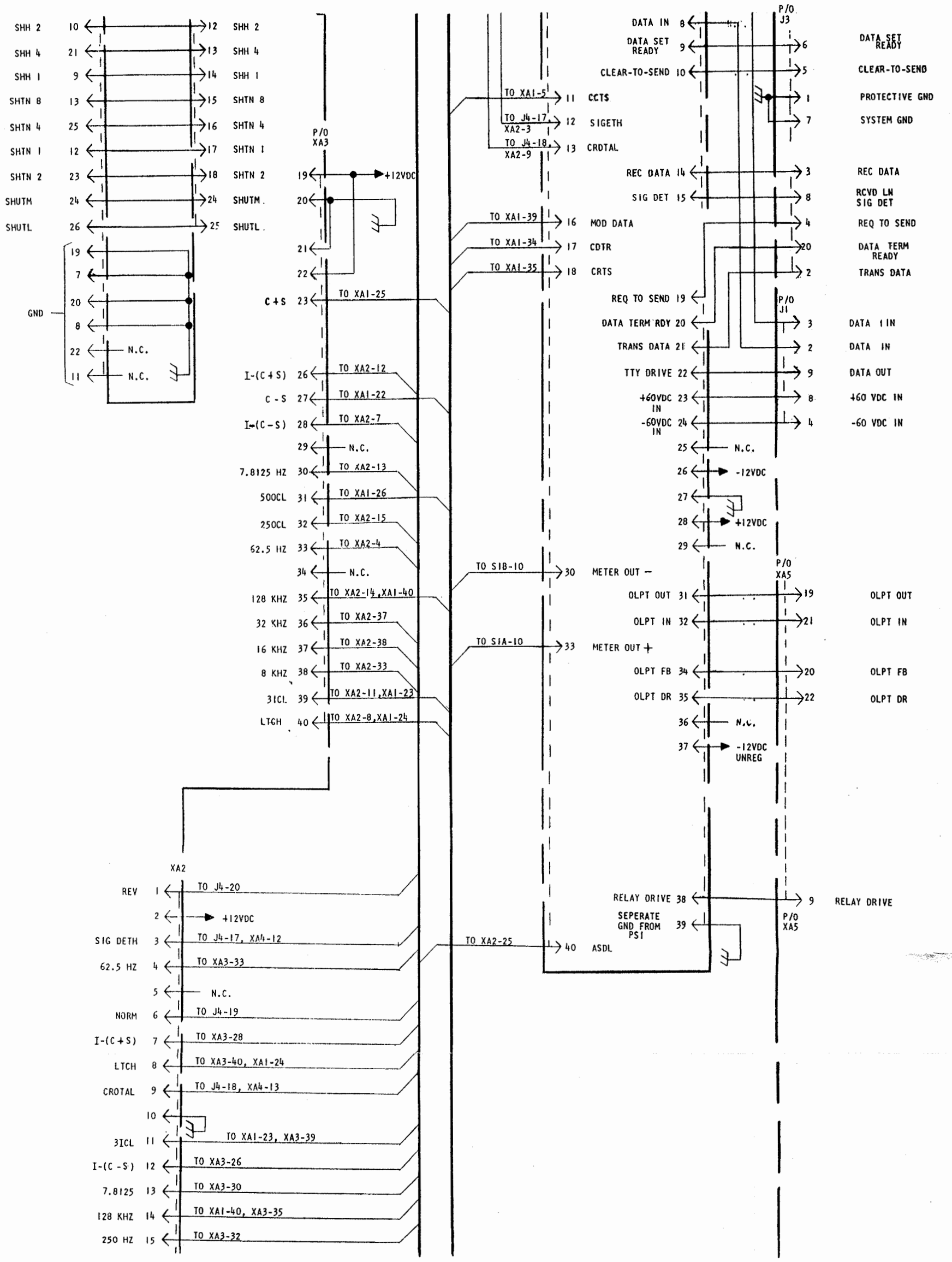


Figure 7-10. Interconnection Pwb W1 Schematic Diagram (Sheet 2 of 3)

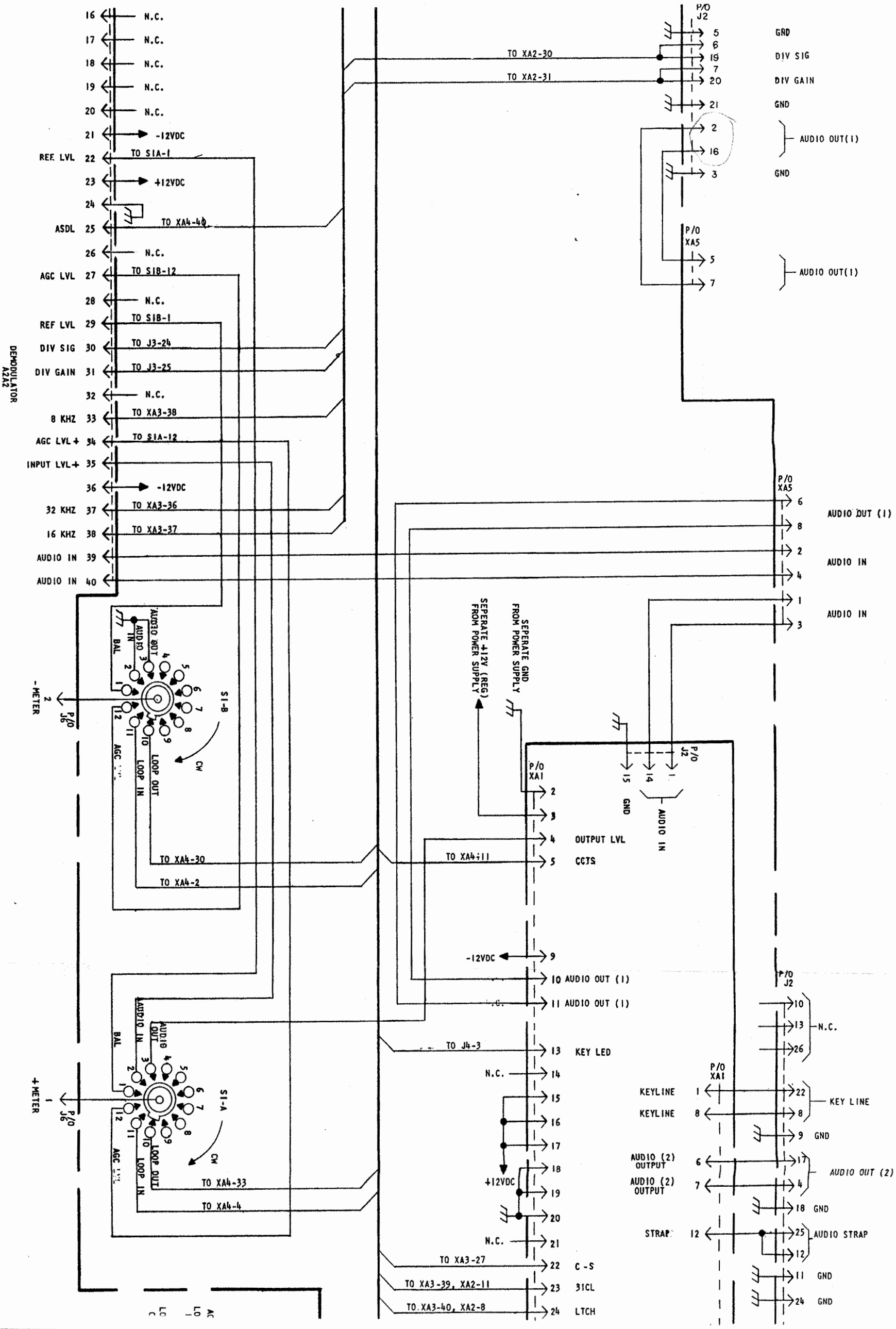


Figure 7-10. In

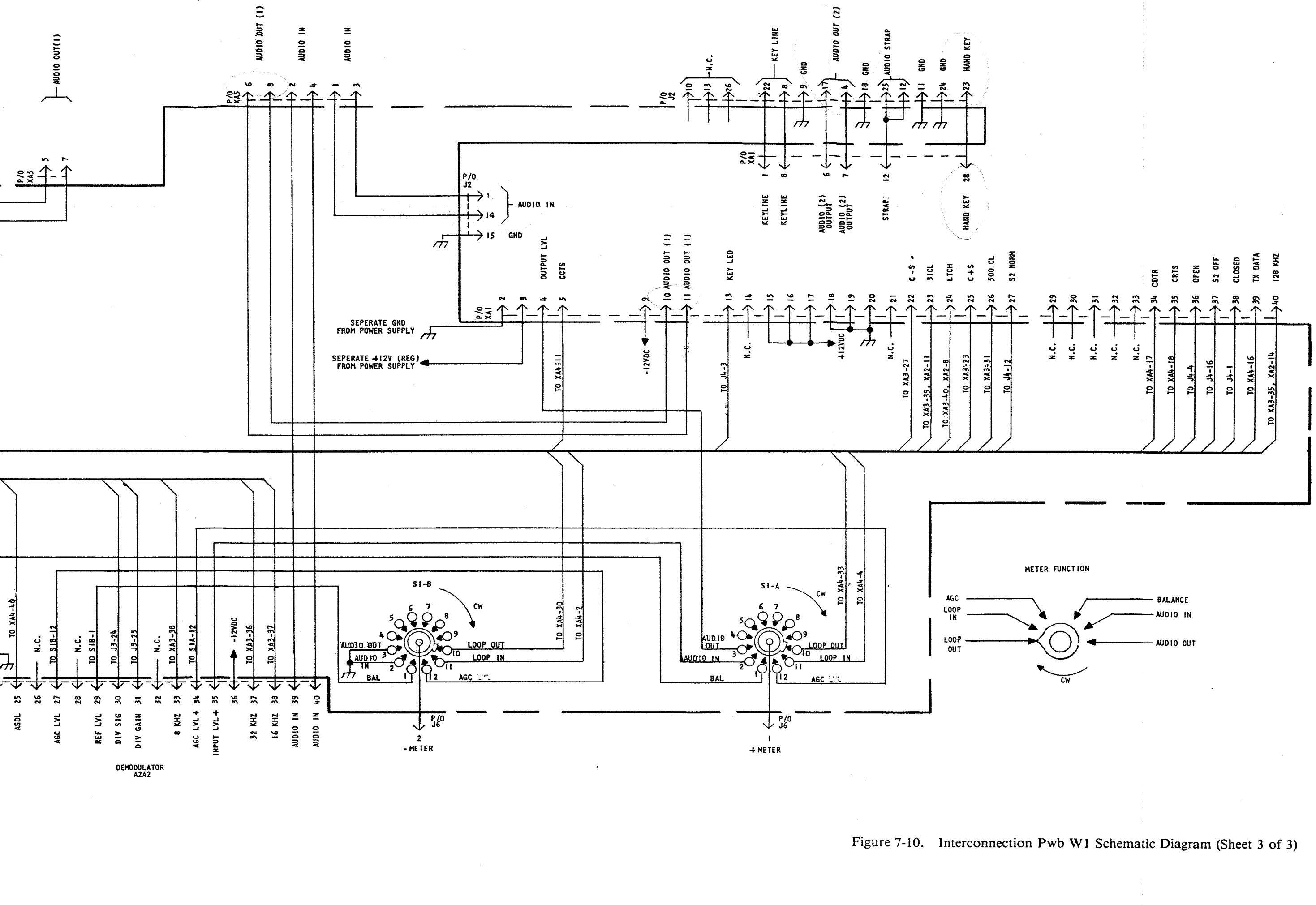


Figure 7-10. Interconnection Pwb W1 Schematic Diagram (Sheet 3 of 3)